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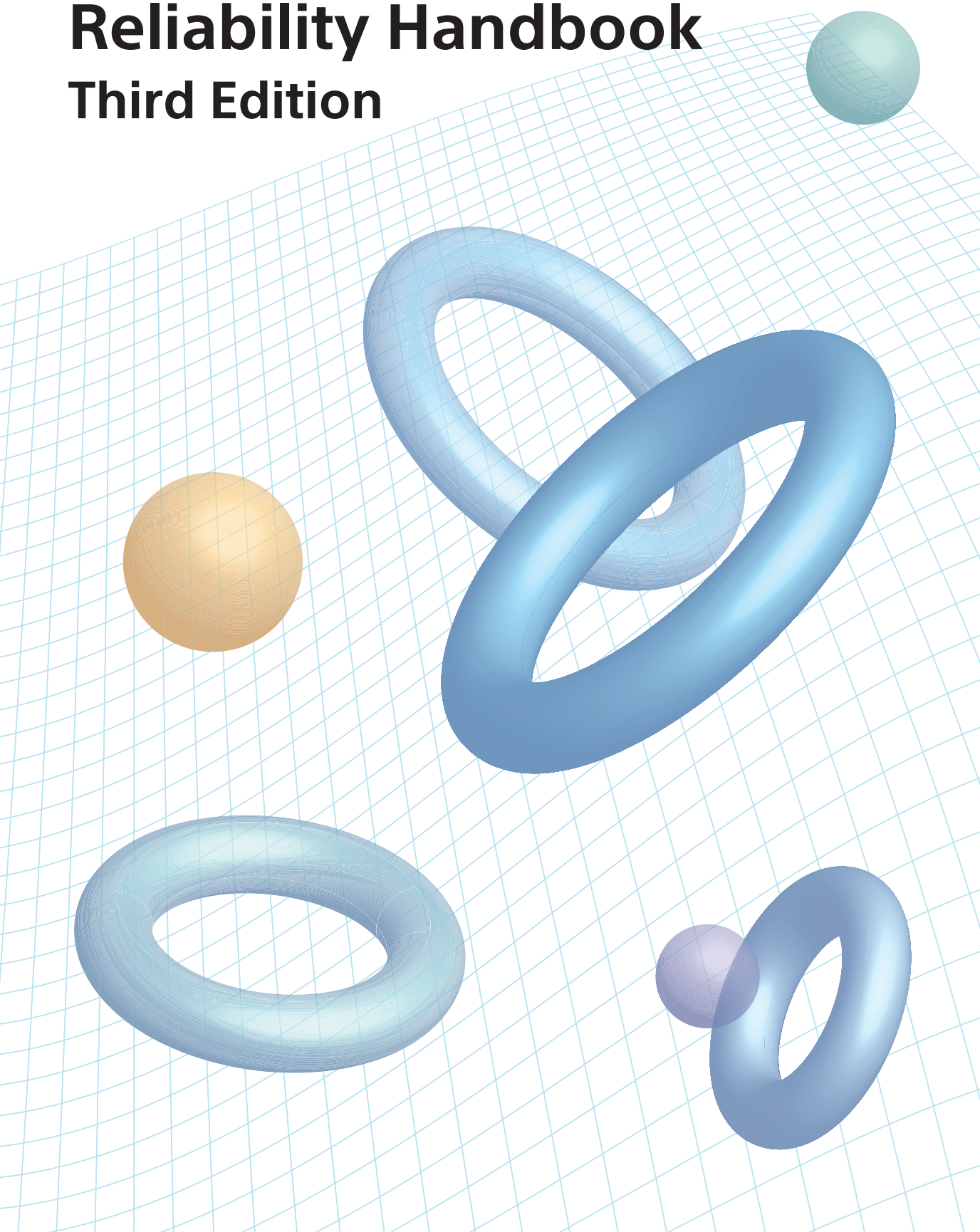
Semiconductor Quality and Reliability Handbook

Third Edition



Semiconductor Quality and Reliability Handbook Third Edition.

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Thank you very much for your continued patronage of our products.

We are pleased to announce that "Sony Semiconductor Solutions Corporation Quality and Reliability Handbook Vol. 3" which summarizes our concept for the quality and reliability of our products and a part of our research and development results has been completed.

At Sony Semiconductor Solutions, we bring semiconductor products that form the basis of key technologies in all industries to our customers through our comprehensive technology of highest quality.

In order to continue to be a reliable device manufacturer for our customers, we strive to ensure high product quality and reliability through consistent quality management system from product planning to design, manufacturing, evaluation and service across all the departments.

"Sony Semiconductor Solutions Corporation Quality and Reliability Handbook" has been prepared with an aim of widely introducing our concept of quality and reliability and precautions on usage of our products to our customers and obtaining their understanding on our products. We would be pleased if you could utilize this Handbook as an aid to improving the quality and reliability of your products and services.

August 2018

Sony Semiconductor Solutions Corporation
Representative Director, President
Terushi Shimizu

At Sony Semiconductor Solutions, we are engaged in our business activities with an aim of contributing to the development of our customers' lifestyle through product development utilizing the latest technology.

Along with the significant changes in our lifestyle such as the introduction of automatic driving and the rapid evolution of IoT technology, the quality and reliability expected of products has become more important than ever.

Against this backdrop, we are working on improving quality and reliability of our products with the focus of contributing to our customers with an open mindset.

In addition to introducing our initiatives outlined above, the Handbook has been prepared with the aim of helping our customers improve the quality of their products and services through the use our products in more accurate ways in terms of quality and reliability.

With this Handbook, we would be pleased if you would understand our stance on the manufacturing activities of providing KANDO (excitement) to our customers through quality and reliability. Once again, thank you very much for your continued support and cooperation.

August 2018

Sony Semiconductor Solutions Corporation
Head of Quality and Reliability Department
Senior General Manager, Quality Reliability Division
Dai Sugimoto

[Notes]

1. This document is written so that it can introduce Sony Semiconductor Solutions' (referred to as "our" hereinafter) efforts for maintaining and managing the quality and reliability of our semiconductors to customers, who already use our semiconductors or are planning to purchase them and they can understand the general precautions on usage of our semiconductors. It is not guaranteed that every effort described in this document is applied to all of our semiconductors uniformly.

2. This document shall neither add description to nor change the agreement made with customers or specifications exchanged between customers and us. The term "quality assurance" described in this document is used to maintain and manage the quality and reliability of semiconductor products, and does not refer to the quality assurance item described in the agreement.

3. We try to improve the quality and reliability of our products. However, it is inevitable that a failure occurs at our semiconductor products with a certain probability. We would like to ask you to pay special considerations to execution of safety design such as retardant design, design for fire spread countermeasure and malfunction preventive design to produce your products so that any malfunction will not cause a fatal accident, a fire or any other social damage.

4. If your product, for example, aircraft/space equipment, medical equipment, on-vehicle equipment or railway equipment, to be manufactured with using our product requires especially high level of quality and reliability, may cause danger to the lives or bodies of people, or is supposed to very likely cause serious property damage, be sure to contact our Sales representative in advance.

5. Do not use any of our products for military purposes. To export our products, permission based on the laws and regulations related to exporting such as the "Foreign Exchange and Foreign Trade Act" and the "U.S. Export Administration Regulations" is required.

6. Technical materials described in this document are used as reference materials only. They do not allow invocation of our or any third party's intellectual property rights or any other rights or use of it. We are not liable at all for violation of any of these rights caused by use of the materials.

7. Since the descriptions of this document are subject to change without notice due to improvement or for any other reason. Check the latest information when you use it.

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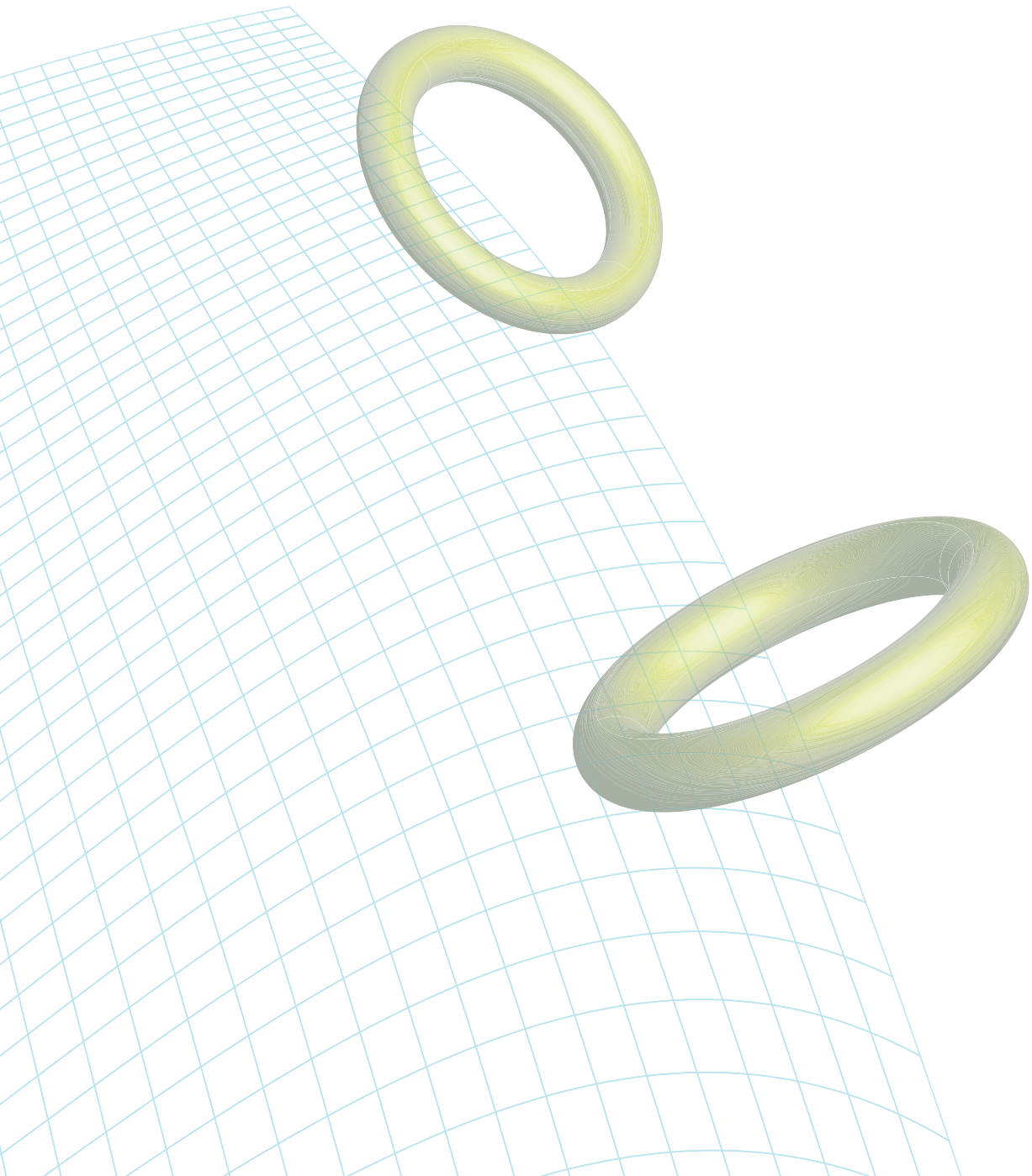

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1.1 Approach to Quality Assurance

1.1.1 Basic policy

We have established the quality assurance system conforming to the IATF 16949 standard as well as ISO 9001, and all our divisions, related departments and factories aim to realize “No. 1 Quality (No. 1 customer satisfaction in the industry with minimum quality losses)” on the basis of values of “Quality First / giving priority to quality over individual profits,” and conduct various quality improvement activities.

1.1.2 Operation of a Quality Management System Based on the ISO 9000 Series

Our quality policy has been established based on achievement of values and vision regarding the quality as follows:

We constantly try to improve the quality of our semiconductor products based on this quality policy through activities such as maintaining and controlling of the quality management system, continuous improvement of the effectiveness of processes, and improvement activities based on quality engineering and other scientific approaches.

Every fiscal year we set goals for customer satisfaction and quality loss, and establish various improvement indexes to realize the “No. 1 Quality (No. 1 customer satisfaction in the industry with minimum quality losses).” We further set the various types of improvement indexes and targets to achieve these goals, and compile various improvement measures for achieving the targets into a quality business plan.

The state of implementation and progress of this quality business plan are reported at quality meetings periodically held by top management, and then reviewed by the top management themselves.

At the Semiconductor Business Unit, we regularly conduct internal quality audits to verify that the product realization plans and practices are in accordance with the quality management system.

In addition, the Sales Department and the Quality Assurance Department communicate with customers and conduct a survey on customer satisfaction to obtain information on how customers think about the quality of our products. We analyze this information to utilize it for customer satisfaction improvement activities.

1.1.3 Method for quality improvement

(1) Sony Six Sigma

Sony Six Sigma was developed based on the Six Sigma developed in the U.S. so that it could be applied to not only product quality but also the quality of all operations. Sony Six Sigma regards the following five as very important thinking ways:

- Customer Focus (Think and judge/act from customers' point of view.)
- Best overall and key thinking
- Focusing not only on results but also on processes to improve variations
- Making objective judgments based on facts and data
- Clarifying return on investment (ROI)

The basic Sony Six Sigma approach is represented by the acronym DMAIC, which stands for Define - Measure - Analyze - Improve (Execute) - Control (Standardize).

In this process, "Define" correctly [defines] action assignments, and "MAIC" [solves] those assignments.

We have deployed this Sony Six Sigma technique to carry out activities aimed at continuous improvement of the "management quality."

(2) Quality engineering

Quality engineering is a specific technical methodology for simultaneously realizing high quality and high productivity, and centers on methods for evaluating and improving functionality. It could be also said that quality engineering is a method for performing "Measure," "Analyze" and "Improve," which are Six Sigma approach, in the technical area.

Evaluation of functionality regards the original function of a product or a system as the essence of the technology, and then evaluates the function and its stability. A function of a product or a system is accomplishing the purpose by converting energy. For example, the function of an image sensor is converting light energy into electrical energy. It is supposed that two or more quality characteristics are necessarily improved when this function is fulfilled enough. Evaluation of functionality represents variations of the function caused by error factors such as differences in a customer's operating and environmental conditions with a unit of measurement known as the S/N ratio. The S/N ratio is calculated based on the ratio of the effective energy representing a function to variations of the function caused by error factors. It can be also said that the S/N ratio is an index for improving many quality characteristics effectively.

A function and functionality can be improved by selecting and combining various technologies, materials, size and creation methods. These choices are referred to as “control factors.” Control factors can be freely selected by us, a manufacturer, within the law. Development and design of a product or a production process are nothing less than good combination of control factors for improving a function and functionality. Parameter design is reviewing of combination of these control factors. Since there are numerous combinations of control factors, generally parameter design is conducted effectively through the experiment plan such as orthogonal table.

Parameter design can not only improve a function or functionality by combining control factors based on the experiment plan but also clarify the control factor effective for improvement. If you find a control factor effective for especially improving the functionality, that is, a control factor effective for variations in a development and design stage, it becomes very useful for securing stability in the market or in the production process.

Since quality engineering is utilized to evaluate whether the technology to be used for a product or a system is appropriate or not and/or the limitation of technology in a short time in advance of product planning, the development period can be shortened drastically through improvement in development efficiency. Furthermore, since the basic power of technology is raised, we can quickly support development of a similar product that utilizes the same technology or the next new product. In addition, the technology becomes very powerful essentially for error factors such as one affecting a customer’s use condition or environmental condition, and this leads to prevention of a failure from occurring in the market or in the production process. Even though a failure occurs, we can support customers immediately because the cause has been clarified in the development and design stage.

(3) Failure Mode and Effect Analysis (FMEA)

Failure Mode and Effects Analysis (FMEA) consists of confirming and evaluating the risks posed by the failure modes that are latent in devices or processes. Confirming these risks makes it possible to systematically discover what is necessary to eliminate or reduce decisive trouble and achieve an optimum design. This analysis is used in 8D Method, which is used to solve a problem of a semiconductor product for a car.

1.2 Quality Assurance System

To ensure quality and reliability and to supply products whose quality and reliability meet customers' needs in a timely manner, all organizations of our company carry out activities based on a consistent quality assurance system, from the product planning conception stage through development, design, manufacturing of prototypes, evaluation, mass production, shipping, and after-shipment activity.

Figure 1-1 shows our company's quality assurance system diagram.

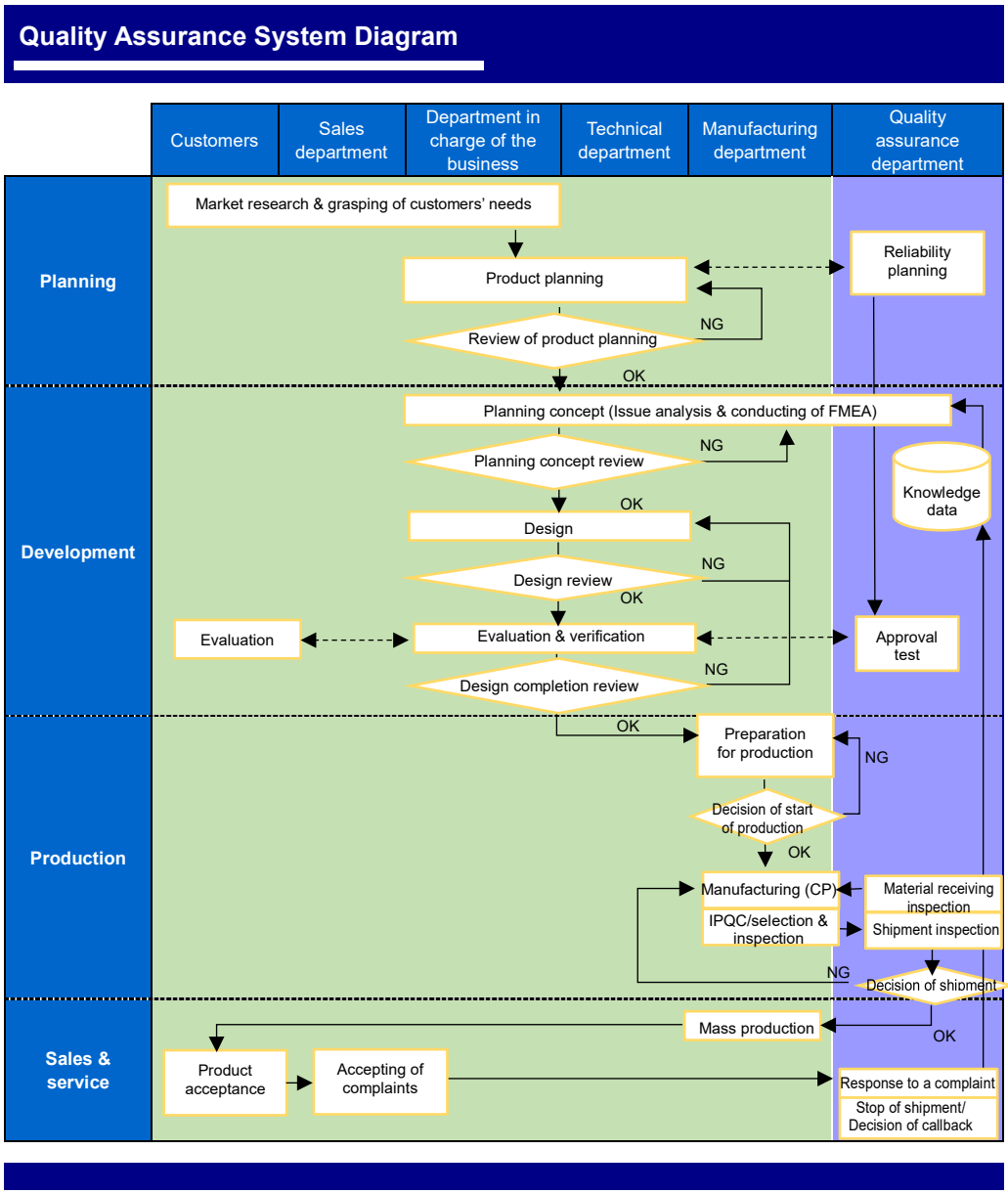


Figure 1-1 Quality Assurance System Diagram

1.2.1 Quality Assurance in the Development and Design Stage

We have established rules for the development and design process and performs operations according to those rules in order to provide customers with same-quality and attractive products that meet the requirements from customers and the market.

(1) Product planning

Market research activities are performed to ascertain the purpose of use, use conditions, and quality and reliability levels required by each customer, and also technical trends, required performance, delivery periods, prices, quality, reliability and other demands on products in the market. This information is used to perform product planning as a product development plan.

(2) Planning conception

The product planning results and various data obtained from quality and reliability results accumulated within the company and obtained from fundamental research on reliability technology are used to set quality and reliability goals that are appropriate for applications and operating environments of products, and to formulate development plans. In addition, based on this quality and reliability information, a plan about the entire design and development process including the product requirements is put together, and then input to designing. In this stage, the related parties including the Quality Assurance department perform FMEA to check and evaluate risks.

(3) Design

Design is an extremely important process for ensuring high reliability of semiconductor devices. Design is performed based on the product requirements with sufficient design flexibility to tolerate variance in the manufacturing process as follows.

- Understanding the latest requirements
  The latest requirements are understood, and all necessary changes from the planning stage are clarified when they should be, visualized (compiled into documents) as the latest requirements, and shared with related parties. In addition, past review analysis results, if any, are also understood as requirements.

- Planning
  The requirements are broken down into specific plans. If any information such as requirements is changed, the necessity for revising the plans is verified. If any plan has to be revised, the plan is updated as appropriate, and the latest version of the plan is visualized (compiled into documents) and shared with all the related parties who will be affected by the design change. Risk countermeasures are also included in these plans.

- Execution
  The corresponding operation is performed in accordance with each plan until we achieve the goal.

- Progress management
  The progress of a plan is managed, and achievement conditions are reviewed to ensure that the expected results are obtained, and all problems are dealt with as appropriate.

(4) Evaluation and validation

The design results are checked to make sure that they satisfy the product requirements (verification) and that the intended applications and purposes are achieved (validity check). This validity check includes reliability certification tests performed by our Quality Assurance Department, and reliability is checked from the standpoint of our customers. Shipment of products to customers cannot start until these verification and validity checks are completed.

(5) Design review

The design results and the compliance state of the design specifications used as the design inputs are checked as the design review. Design review is carried out even in the middle of the design work, if necessary, and these results are fed back to the design to improve design quality.

In design review, during circuit design, layout design, wafer process design and assembly process design, whether the design complies with the design standards, which are the rules to be followed, is checked and design contents are thoroughly investigated by technical experts. Furthermore, experts from the related departments review design contents from the viewpoint of cases of past trouble and/or technology unique to each of them. These design reviews aim to avoid a failure/trouble after prototype creation and mass production, and build the target performance, quality and reliability into products as demanded.

1.2.2 Quality Assurance in the Mass Production Stage

(1) Process quality control in manufacturing

In order to timely provide the high reliability and high quality products that meet the customers' needs, the related departments perform capability verification with respect to production, shipping and material purchasing plans that have been made based on the latest sales plan, and then operations shift to the production stage.

Based on the concept that high quality should be achieved in the manufacturing process, the manufacturing conditions that have been determined according to the various drawings presented by the Development Design Department are stipulated in control plans (descriptions or systemization of the process flow, equipment to be used, equipment handling procedures, work conditions, work methods, parts and materials to be used, parts and materials handling methods, various QC items and control criteria, inspection criteria, definitions of troubles and methods for dealing with them). These control plans are then compiled into documents and used as guides for performing each manufacturing operation. In addition, we use the SPC(Statistical Process Control) method and other tools to detect changes in important control items that have a significant effect on quality and reliability, and try to stabilize quality and to discover a trouble in the early stages and prevent it from occurring.

Also, all necessary information on quality from purchasing of materials and parts to quality control of the manufacturing process, inspections, warehousing and shipment information for customers is controlled and analyzed by a data collection system and used to improve the quality.

In addition, this information is also used to quickly identify the range affected if any trouble occurs by any chance.

If any trouble occurs in the manufacturing process, a trouble report is issued, the Technical Department in charge investigates the trouble, and then the corresponding necessary corrective action is taken to prevent the trouble from occurring again.

Whether products manufactured in this manner satisfy the product specifications and customer demands is checked during a final inspection process, and only accepted products are shipped to customers.

(2) Process quality control of outsourcing contractors

Even when a part of the manufacturing process is outsourced, quality assurance activities are promoted for outsourced production lines based on the same approach as our in-house line. These activities include product quality assurance, process control, quality improvement activities and corrective actions for troubles, and we try to maintain and improve product quality and to prevent a trouble from occurring.

Manufacturing line audits are conducted by specialists including Quality Assurance Department members as main members when outsourced production starts to make sure that there is not any problem.

In addition, we evaluate the reliability of outsourced products in the same manner as our own products to make sure that there is not any problem.

(3) Statistical process control (SPC)

The manufacturing process is controlled with a check sheet, a graph and/or a control chart. Especially a control chart is used as an effective method for monitoring change in the quality of each process continuously and allowing us to take an appropriate action for a trouble.

In a control chart, the control limit showing the normally obtained data range based on variations of a certain range of process data is set, and the measured data is written on the chart.

If an unordinary factor is shown in variations of the process, some data exceeds the control limit line: this is effective to detect change in the process at an early stage. In addition to this deviation from the control limit, we can detect change in the process from the data upward/downward tendency. In this way, statistical methods such as a control chart are used to find variations affecting the quality on a regular basis, and analyze them to improve the quality.

Important control items are decided based on items that affect the quality reliability of devices and items correlated with a mechanism of defective occurrence besides characteristic items required by customers. Based on these important control items, each process capability index (Cp, Cpk) is calculated. When the process capability index of a control item is low, we improve the corresponding process, and try to raise it to the higher level to realize the stable quality.

(4) Measuring instrument control and environment control

During semiconductor development design and production, product performance and quality are assured and improved when measuring instruments constantly operate in the normal condition and within the required accuracy. To control the accuracy of measuring instruments,

we conduct receiving inspections when purchasing measuring instruments, run periodic checks when the instruments are used in order to check the accuracy of the instruments, and periodically calibrate them. By performing these operations, we have established the preventive maintenance system to prevent the instruments from malfunctioning or their accuracy from being lowered.

The environment has a significant effect on the quality reliability of semiconductor devices. Therefore, we set control items, control methods and control standards for temperature, humidity, dust and other items according to the manufacturing process and micro-machining level, and maintain and control the environment by installing a centralized monitoring system or similar system. In addition, the quality is also maintained and controlled by monitoring the resistivity, purity and other characteristics of the deionized water, gases and chemicals used in manufacturing in-house production lines.

(5) Product traceability

As for traceability of products shipped to customers, the mark lot number printed on the final product is used as the key, and this mark lot number is associated with the used parts and materials lot and the manufacturing history. The product name and mark lot number of the enclosed products are described on the label pasted on the outside of the packing carton, so that the manufacturing history can be traced even when a product is packed in the package.

1.2.3 Change Control

Semiconductor products or manufacturing processes are changed in order to improve their functions, quality reliability and also productivity. We determine whether the product or manufacturing process can be changed after confirming that the change will not produce any negative effects in all aspects. In addition, when a change is planned, the related departments review the change. The necessary and optimum evaluation of items supposed to have a technical effect is planned, and these effects are checked by manufacturing prototypes or another method. If the changed product has a significant effect on customers, we contact the customers based on these evaluation results in advance. After we gain agreement with them on the change, we start delivering the changed products to them.

1.2.4 Quality Assurance of Purchased Products (Materials and Parts)

As the reliability and the density of semiconductor devices become higher, the required quality level of purchased products is also becoming higher. It is needless to say that the quality of purchased products is important to assure the quality of semiconductor devices. We put in writing the system for purchasing parts that covers evaluation, selection and registration of suppliers, production line certification, exchange of specifications, receiving inspections, materials and parts inventory and control, and promote quality assurance activities based on these documents.

(1) Evaluation, selection and registration

The Purchasing Department together with the Technical Department and the Quality Assurance Department evaluates the “Management conditions,” “CSR (Corporate Social Responsibility including law compliance),” “environmental considerations (application of the Sony Green Partner System),” “technical capability,” “cost,” “quality” and “supply capability” based on the

functions and performance required for the purchased parts to select new suppliers, and registers suppliers who meet the criteria.

(2) Production line selection

Mainly the Purchasing Department, the Quality Assurance Department and the Technical Department review the “Quality management systems,” “process quality control” and "technological responsiveness" and certify the production lines of suppliers that have come up to the given standards.

(3) Exchange of specifications

After finishing evaluating (function characteristics and quality reliability) of the purchased parts, the Technical Department creates specifications. After the Purchasing Department exchanges these specifications with the suppliers, it assigns a unique number to each purchased part, and registers and controls it.

(4) Monitoring and management of suppliers

The Purchasing Department obtains information on QDCS results from the related departments of the suppliers with whom we continuously do business to periodically evaluate these suppliers. We give appropriate instructions to suppliers based on these evaluation results to accelerate the quality improvement activities of suppliers.

(5) Change control of purchased parts

After the Purchasing Department receives the applications for changes, the related departments such as the Technical Department and the Quality Assurance Department verify them. Changes are made only when the verification results indicate that there is no problem, and traceability related to the changes is allowed securely.

1.2.5 Coping with a Malfunction

If a trouble occurs at a customer’s site, the Quality Assurance Department accepts information on the trouble via a special sales agent or the Sales Department. Investigation and analysis of a malfunctioning product and feedback of the results are both a duty and a service to customers, and at the same time offer valuable information for improving product quality.

Investigation result of a malfunctioning product and the corresponding corrective action are reported to customers in document form and we may visit customers to report these results to them directly depending on the situation so that they can understand the result and the corrective action.

(1) Trouble information

The more accurate information is provided, the more easily the investigation and analysis can proceed in order to deal with a trouble quickly and securely when it occurs. Therefore, when customers request investigation of a malfunctioning product, they are requested to present detailed information such as information on the trouble, the process in which the trouble occurred, the electrical, mechanical and thermal stress application history, lot dependency, trouble occurrence rate, conditions of the surrounding circuits and applications. Especially if a lead is bent or a packing failure occurs (for example, an incorrect item is packed or a different type of part is packed), the detailed information obtained when the trouble occurred is required.

(2) Return of a malfunctioning sample

A malfunctioning sample has to be returned in the condition in which the trouble occurred wherever possible. When returning a sample to us, a customer is requested to take appropriate measures to avoid external stress (electrical, thermal, mechanical and/or electrostatic) so that the effects of such stress will not change the malfunctioning conditions during handling and transport.

(3) Corrective action

After identifying the cause based on the investigation and analysis results of the malfunctioning product, we take the measures for the trouble, and then a corrective action for the quality management systems in the applicable process to prevent the trouble from occurring again.

1.3 Management of Outsourcing Contractors/ Physical Distribution Quality

1.3.1 Management of Outsourcing Contractors

We try to improve the quality of the outsourced business and secure the quality of products provided by an outsourcing contractor through selection of an outsourcing contractor and execution of the outsourcing contractor management process described below in order to provide customers with high quality and high reliability products.

(1) Selection of an outsourcing contractor

When we have to select a new outsourcing contractor, the department in charge of the outsourced processes collects information on the target outsourcing contractors, for example, by investigating their business results and the industry trends to select candidates to whom a process is to be outsourced. Next, depending on a process to be outsourced, the department in charge of the outsourced processes investigates these candidates, collects information on them, analyzes the information together with departments in charge of the quality, business, technology and purchasing respectively to make the overall assessment based on the evaluation results of each department, and then decides the optimum outsourcing contractor. (See Figure 1-2 Outsourcing contractor selection flowchart.)

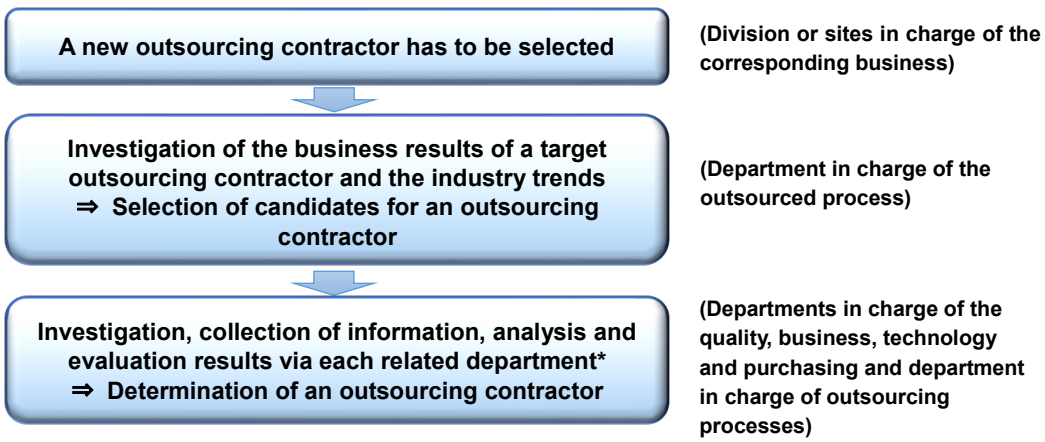


Figure 1-2 Outsourcing contractor selection flowchart (example)

* Outsourcing contractor evaluation items (example)

1) Financial condition, whether an outsourcing contractor can undergo an audit and response to CSR (Corporate Social Responsibility)
2) Environment management capability for Green procurement (check to see whether an outsourcing contractor has been certified as our Green partner)
3) Quality assurance capability of a process to be outsourced (check to see whether a production line of an outsourcing contractor has been certified)
4) Technological capability for executing a process to be outsourced and handling capability of workload to be outsourced

(2) Management of outsourcing contractors

① Management of outsourcing contractors

We manage an outsourcing contractor (manage items such as progress, quality, delivery date, risk and improvement) so that products can be delivered to us as regulated on an order form. The department in charge of outsourced processes determines the degree of management of an outsourcing contractor and how to manage it with taking into consideration its quality level, how a quality problem has occurred at its site if any and how much the problem has affected its products for each order by reference to the following items. (See Figure 1-3 “Outsourcing contractor management example.”)

1) To carry out monitoring and measurement using management indicators to ensure the quality of deliverables of outsourcing suppliers and implementation of planned work
2) Check of the quality state of an outsourcing contractor through a periodic meeting with an outsourcing contractor
3) Check of the quality state with a periodic report submitted by an outsourcing contractor
4) To visit outsourcing suppliers to provide them with on-site guidance and to confirm quality information
5) To confirm quality by verifying deliverables of outsourcing suppliers

② Continuous evaluation of an outsourcing contractor

In order to secure the quality of an outsourcing contractor’s operation process and products (output), the department in charge of outsourced processes cooperates with the departments in charge of the quality, technology and purchasing to evaluate the business performance of an outsourcing contractor once a year. The department in charge of outsourced processes determines evaluation items by reference to the following:

1) Financial condition (including the procurement environment changed according to change of the financial condition)
2) Quality state (State of the quality of a process to be outsourced such as product quality, design quality and manufacturing quality)
3) On-time delivery state
4) Cost and cost reduction condition

③ Change control

When the department in charge of outsourced processes requests an outsourcing contractor to change the specifications or when the contractor requests change of the specifications, it cooperates with the related departments (such as the quality department and the technical department) to evaluate the change thoroughly so that it cannot have any adverse impact on the quality of a product or conformance to the environment of the product to decide whether the change can be accepted.

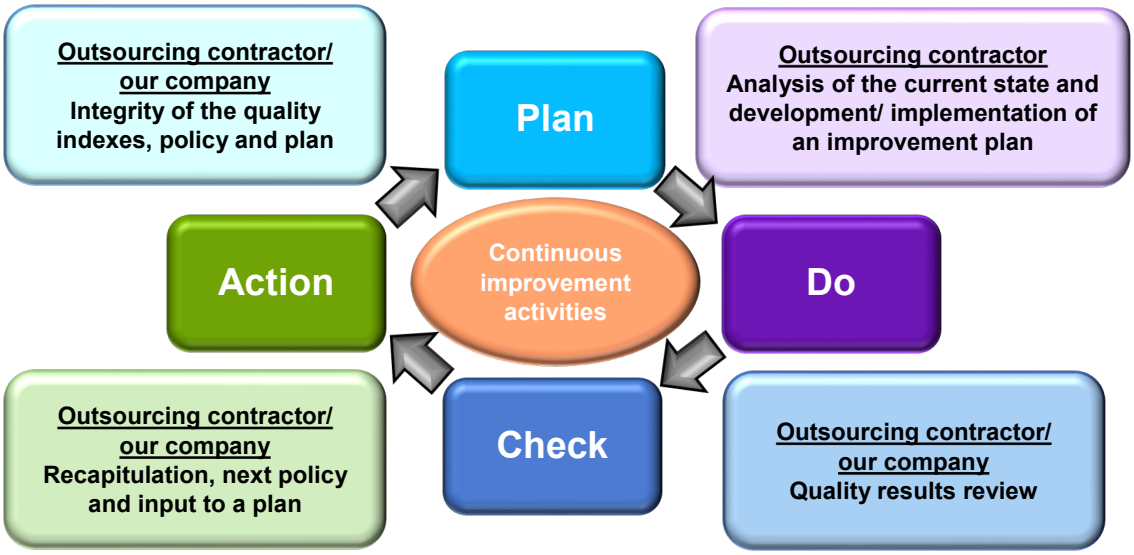


Figure 1-3 Outsourcing contractor management (example)

1.3.2 Logistics Quality

We make efforts for the logistics quality assurance in the logistics process together with the Device Sales Department, the Quality Assurance Department, the Sales company/special sales agents and the physical distribution base cooperatively to provide customers with the quality of products (including packaging specifications) realized in the Manufacturing Division.

(1) Basis of the quality assurance of the logistics

Figure 1-4 shows the outline of the logistics quality assurance system.

Responsibility of the logistics quality lies with the Device Sales Department, and the sales company/special sales agents under the control this department appoint persons in charge of the logistics quality to control the physical distribution base practically. In addition, the Quality Assurance Department to which the quality assurance authority is delegated monitors the logistics quality; mainly approves the logistics quality.

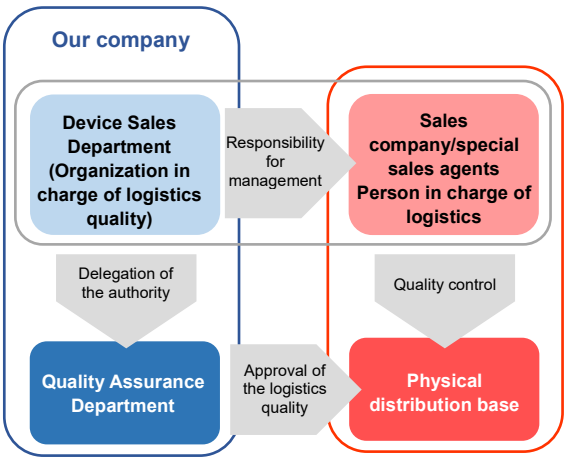


Figure 1-4 Logistics quality assurance system (overview)

(2) Approval of the logistics quality

Figure 1-5 shows the conceptual diagram of the logistics quality approval and logistics audit, both of which are fundamental part of the logistics quality assurance.

To guarantee the logistics quality, a system for maintaining the logistics quality in conformance to the requirements regulated by the Quality Assurance Department has to be established and maintained at the physical distribution base, and operated under the appropriate control.

The Quality Assurance Department decides whether to approve the logistics quality based on the audit results aiming at validation of this system. When it approves a physical distribution base, it gives the corresponding certification to the physical distribution base to allow the base to ship products. The certification is valid for one year when it is given to the physical distribution base for the first time. It becomes valid for one year and a half after that although the base has to receive an audit for updating the certification.

Approximately 20 bases of 7 sales companies and approximately 20 bases of special sales agents are to be approved over the world.

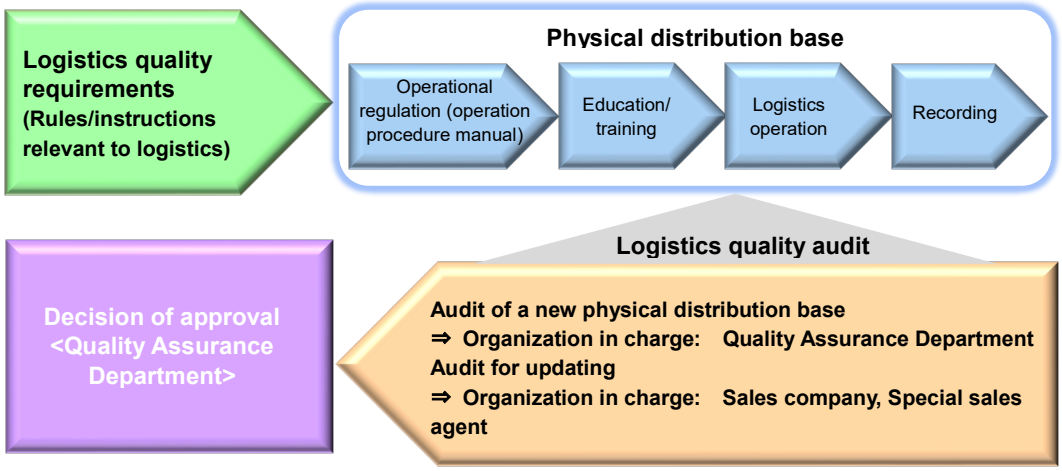


Figure 1-5 Logistics quality approval and audit

(3) Audit of logistics quality

We carry out the following measures to secure the quality of logistics quality audits to be conducted at approximately 40 bases over the world and for audits to contribute to improvement of the logistics quality.

a) Certification of a lead auditor

A lead auditor has to take the training provided by the Quality Assurance Department and pass the examination. After he/she takes up the post of a lead auditor, he/she shall accept the inspections to be conducted by the Quality Assurance Department periodically.

b) Audit plan and results

When an audit starts, the Quality Assurance Department regards the detailed control items shown in Table 1-1 as the requirements, and summarizes them in a check sheet configured of 100 or more requirement items to present the sheet to each sales company and each special sales agent. The department presents the important check items for the audit to the sales companies and special sales agents also. In response to this, a lead auditor has to add a specific check target(s), his/her own check items and check targets to the check items of the check sheet. When the Quality Assurance Department approves the check sheet to which the lead auditor adds these descriptions, an audit starts.

The lead auditor summarizes the audit results as a report, and then the Quality Assurance Department has to examine the report closely, and then approve it.

Table 1-1 Control items of the logistics quality

① Product handling control
② Statistic electricity control
③ Product storage control
④ Corresponding to environment
⑤ Control of an operation failure
⑥ Response to a disaster/accident
⑦ Management for special adoption
⑧ Logistics evaluation and monitoring
⑨ Document control and recordkeeping

c) Corrective actions

If an audit detects any unacceptable matter, the corresponding physical distribution base creates a corrective action plan, and then takes the action after the Quality Assurance Department approves it. The lead auditor checks the result of the corrective action and the matter at the site, and then the Quality Assurance Department approves the result if it is appropriate.

Until the corrective action is taken completely, the corresponding physical distribution base cannot obtain the logistics quality certification, and cannot ship any product.

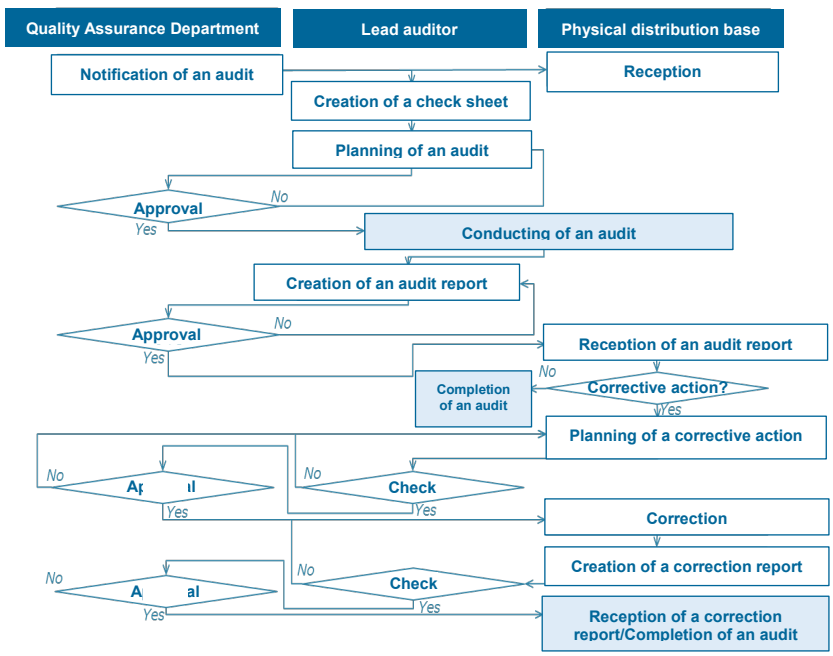


Figure 1-6 Basic flowchart of a logistics quality audit

1.4 Environment

1.4.1 Efforts for Environmental Protection

1.4.1.1 Sony group environmental vision

Sony formulated the “Sony Global Environmental Vision” consisting of a “Philosophy” and “Principles” as the global environmental policy for the entire Sony Group to aim for realization of a sustainable society.

In 1993, Sony formulated the “Sony Global Environmental Policy” and Environmental Action Program, which are the predecessor of the “Sony Global Environmental Vision,” and has continued the environmental activities.

Our company also has worked in the same manner as one member of the Sony Group. The Sony’s “Philosophy” and “Principles” are described below.

1.4.1.2 Philosophy

Sony recognizes the importance of preserving the natural environment that sustains all life on the earth for not only now but also future generations and thereby ensuring that all humanity can attain a healthy and enriched life. In order to realize such a sustainable society, Sony strives to reduce environmental burdens to zero throughout the lifecycle of its business activities and its products.

1.4.1.3 Principles

Sony makes efforts to reduce environmental loads surely and prevent environmental pollution throughout its business activities and the entire lifecycle of its products and by complying with applicable environmental regulations and also by continually improving its global environmental management systems. Sony formulates the following goals in four key environmental perspectives and takes proactive actions to achieve those goals.

(1) About climate change

Sony reduces energy consumption and aims to achieve zero emissions of greenhouse gases generated throughout the lifecycle of its products and services as well as its business activities.

(2) About resources

In order to minimize new input of resource to Sony’s business activities, Sony identifies “Key Resources” and aims to achieve zero usage of these new materials. Sony also tries to use water efficiently, minimizes wastes from its sites, and makes every effort to collect products from the markets and recycle them.

(3) About chemical substances

Sony minimizes the risk of used chemical substances causing serious harm to human health and the global environment. Sony not only takes secure control over the used substances but also tries to continuously reduce and substitute substances that have potentially significant impacts on the environment from the point of view of preventive measures, and stops using such substances whenever it becomes possible even in the cases where scientific evidence is not fully proven.

(4) About biodiversity

Sony actively promotes maintenance and recovery of biodiversity through its business activities and local contribution activities to try to preserve and utilize ecosystem services in a sustainable manner.

1.4.2 Environmental consciousness at the sites

We promote the activities for reducing environmental loads such as energy saving at the related sites according to the Sony Group Environmental Medium-term Goal “Green Management 2020.”

Furthermore, we develop the regional activities focusing on contribution to the environment in response to local needs (including the activities for environmental conservation inside the sites).

(1) Reduction of the total greenhouse gas emissions

We are making efforts to reduce greenhouse gas emissions such as carbon dioxide (CO_2) generated due to use of energy and perfluorocarbon (PFC) used in a manufacturing process. We also promote cyclic use of energy such as installation of high efficiency apparatus and recycling of exhaust heat generated by air-conditioning equipment in semiconductor clean rooms. We implement measures to reduce greenhouse gas emissions such as PFC by installing processing equipment.

(2) Reduction of water usage

In the manufacturing processes, we use pure water purified from well water or industrial water for many purposes: cleaning of semiconductors and cooling of devices. To conserve water resources, we implement measures to reduce the amount of used water by collecting it, purifying it, and then reusing it as well as trying to reduce the amount of water used in the manufacturing process.

(3) Reduction of quantity of generated waste

To reduce waste such as sludge generated in processes including the chemical treatment process and waste liquid discharged in the manufacturing process, we make efforts to use resources efficiently.

(4) Reduction of volatile organic compound (VOC) emission

We switch the related materials to alternative ones and take measures for reducing the amount of VOC used in the manufacturing processes. We also have developed a small type VOC processing device in conjunction with a device manufacturer and promote its installation.

(5) Environmental regional contribution activities

We hold a communication event (such as cleaning activities) at our sites and actively participate in local events (such as a tree planting activity) too. In addition, we hold a tour to which staff members of regional administration and local residents are invited and a tour useful for environmental education for students of a nearby elementary school so that they can understand our efforts for the environmental problems and can be reassured about the environment.

1.4.3 Control of chemical substance of products

We comply with the laws and regulations regarding chemical substances contained in products, and control the specified environment-related substances to be controlled based on the Sony Group unified standards “Management Regulations for Environment-related Substances to Be Controlled Which Are Included in Parts and Materials (SS-00259)” to reduce impacts on the global environment.

1.4.3.1 Global development of Sony’s unique chemical substance control standard

Electronics products manufactured/sold by Sony contain between a few hundred and a few thousand parts that are made of a variety of chemical substances.

Some of these chemical substances may be classified as hazardous and may harm the environment if they are not properly controlled prior to disposal of products.

To prevent the environment from being polluted in such a way, the RoHS Directive[*1] prohibits certain chemical substances from being contained in products in the EU. In Japan, information on products containing a certain chemical substance(s) are required to be disclosed by a J-Moss mark[*2], while in China, it is required to disclose information on chemical substances contained in products in line with the “Management Methods on the Pollution Control of Electric Information Products,” often referred to as the China RoHS[*3].

In line with the globalization of the products market and the supply chain, Sony has established its own standards for management of chemical substances, “Management Regulations for Environment-related Substances to Be Controlled Which Are Included in Parts and Materials (SS-00259)” [*4], with taking into consideration the related laws and regulations around the world and reflecting the opinions of stakeholders. According to these standards, Sony takes globally consistent control of chemical substances for parts and materials configuring its products.

*1 RoHS Directive regulates the restriction of the use of certain hazardous substances in electrical and electronic equipment. It was implemented in 2006, and revised in 2011.

*2 J-Moss is an abbreviation for the JIS Standard “The marking for presence of the specific chemical substances for electrical and electronic equipment.”

*3 “Management Methods on the Pollution Control of Electronic Information Products,” which is referred to as China RoHS, was implemented in July 1, 2016. It regulates six substances such as lead and mercury contained in electric and electronic equipment to be sold in China.
This regulation requires “products to bear an electric and electronic equipment pollution control mark,” and “information on the contained chemical substances to be disclosed.”

*4 “The Management Regulations for Environment-related Substances to Be Controlled Which Are Included in Parts and Materials (SS-00259)” regulates the standards for giving directions to suppliers about chemical substances for items procured by Sony. These standards classify the usages of the target chemical substances into several categories: those that are prohibited immediately, those that are prohibited after a certain date, and those that are to be prohibited on a not fixed date in the future. (Refer to the “Management Regulations for Environment-related Substances to Be Controlled Which Are Included in Parts and Materials (SS-00259)” for details.)

https://www.sony.net/SonyInfo/procurementinfo/ss00259/index.html

1.4.3.2 Coping with the regulations for chemical substances in products

Sony has established the system for coping with the REACH regulation[*5] and the revised RoHS Directive in the EU. To respond to the articles “Duty to communicate information on substances in articles” and “Registration and notification of substances in articles” of the REACH regulation and the CE marking of the RoHS directive, Sony uses chemSHERPA[*7], which conforms to IEC 62474[*6]. This scheme allows us to collect data on certain chemical substances contained in parts and materials purchased from suppliers and control this data in a database.

*5 REACH (Registration, Evaluation, Authorization and Restriction of Chemicals) regulation is a new control system of chemical substances in Europe, and started being enforced in June 1, 2008. This regulation imposes duties such as registration, application for approval, notification, usage restrictions and information communication on business operators under the specified conditions.

*6 IEC 62474 is the international standard regulating information communication such as the procedure, contents and format for the supply chain of chemical substances and constituent materials of products in the electric and electronic industry, and it was issued in March, 2012.

*7 chemSHERPA is a common scheme for communicating information on chemical substances contained in products that can be used in the entire supply chain. At the initiative of the Ministry of Economy, Trade and Industry, this scheme started to be reviewed in 2013, and then data creation assistance tool was released in October, 2015, and started to be used.

1.4.3.3 Three core principles for managing chemical substances contained in products

To conform to Sony’s own chemical substances control standards, “Management Regulations for Environment-related Substances to Be Controlled Which Are Included in Parts and Materials (SS-00259),” Sony has established three basic principles, and then controls these substances based on these principles.

(1) Upstream management

In 2002, Sony established the “Green Partner Environmental Quality Approval Program,” which clarifies “Sony's Green Partner Standards” necessary for chemical substance management. Sony audits suppliers based on these standards. Sony purchases electronic parts only from suppliers who have passed this audit and have been certified as “Green Partners.” Sony also applies the similar program to contract manufacturers to control chemical substances thoroughly. To further enhance the efficiency of the chemical substances control, in autumn 2003, Sony introduced the “Green Book,” a raw materials database, which is made available to Sony's direct suppliers (tier 1 suppliers) via its electronic procurement system.

In the “Green Book,” Sony has registered only those materials that it has checked, measured and confirmed compliance with the SS-00259 standards for Sony's designated raw materials such as recycled resins and wires, and also for molding resins, paints, inks, and other materials that are commonly used by multiple tier 1 suppliers. To assist REACH compliance, Sony has started disclosing data on the amount of chemical substances contained in raw materials to its suppliers and contract manufacturers.

(2) Management in quality control processes

New parts and materials are tested to ensure conformity with SS-00259 standards in addition to compliance with conventional quality control standards based on the collected data on the amount of chemical substances in parts and materials. By implementing these management procedures worldwide, Sony controls the quality of its product thoroughly so that incompliant products can be prevented from entering the market.

(3) Utilization of chemical analysis

To prevent prohibited substances from accidentally entering products, Sony requires suppliers to conduct ICP (Inductively Coupled Plasma) analysis on the certain parts and materials.

For some high-risk substances, Sony has also implemented internal control systems that involve usage of, for example, X-ray fluorescence (XRF) and other measurement devices, to Sony’s sites worldwide, to confirm that prohibited substances are kept out of products.

1.5 Safety

Our semiconductors are designed for not only consumers' products such as an LSI and an image sensor mainly but also a product lineup designed for a wide range of application such as in-car use requiring higher quality and safety.

We make various efforts for all product lineups to secure the quality and safety required for each product and to continue to provide customers with semiconductors that can be used securely and safely.

1.5.1 Approach to safety

Not only efforts made in the design and development stage but also those in the manufacturing stage are important to improve the safety of products.

We reduce risks through the safety-conscious design from the planning stage with considering troubles that occurred outside the company and high-level mass-production control in the manufacturing stage as described in Section 1.2.2 of this Chapter.

When we select materials, we regard their safety as an important element, and validate it based on the evidence also.

In this way, we link validation performed in each process to the next process from development to control of mass-production to make efforts to produce safe and high-quality products in a consistent way.

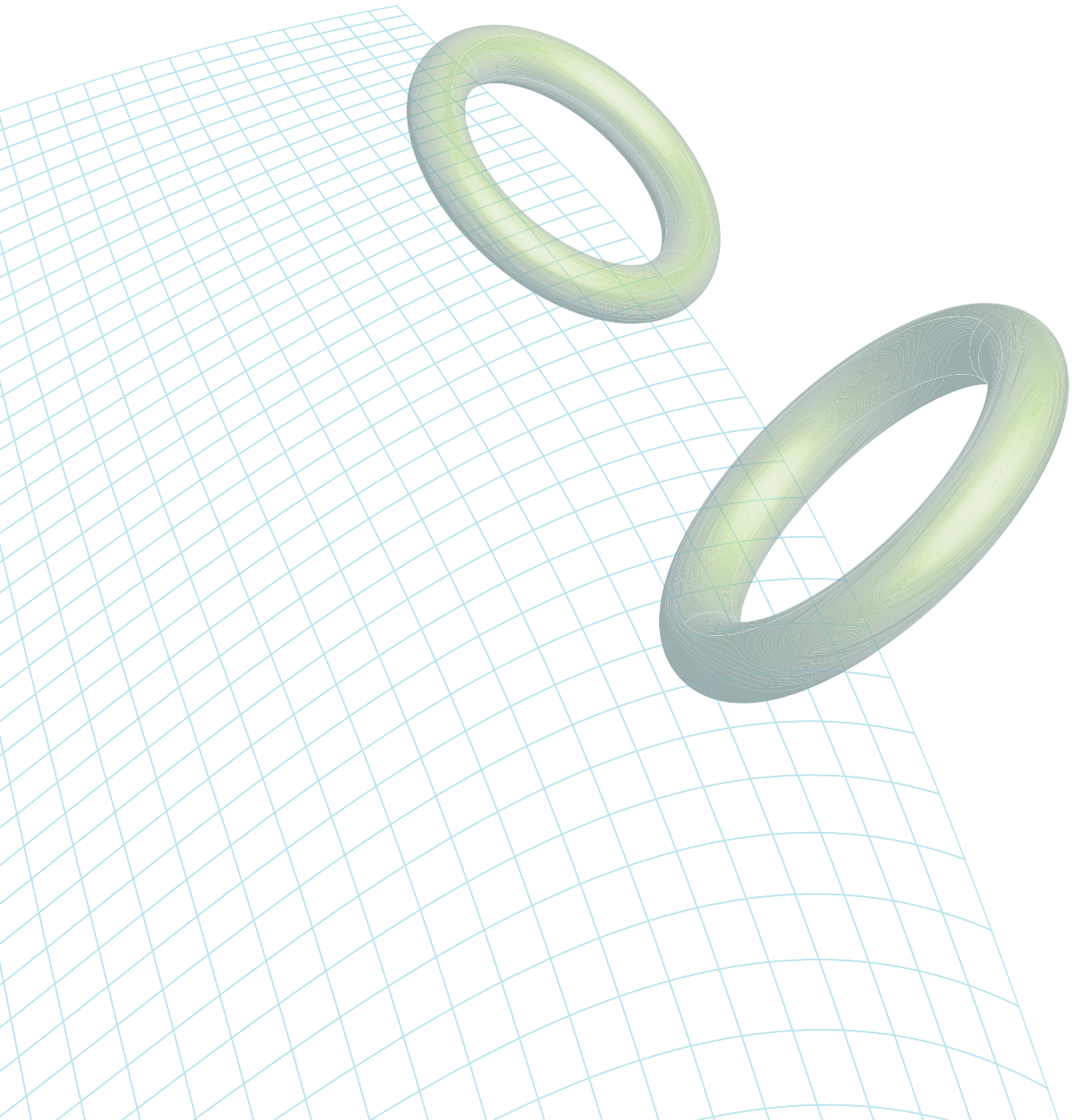
1.5.2 For safe use of products

As described above, we securely provide customers with products via various efforts. Therefore, we ask customers to use our products correctly.

We hope that customers will understand the specifications of products such as a product specification document, and pay attention to safety from when they select a semiconductor until when they use it.

* See the Chapter 6 "Notes on Handling of a Semiconductor Device" for details.

Chapter 2 Quality of Automotive Semiconductor Products



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2.1 Our Automotive Semiconductor Products

Although Sony has a strong image of consumer products, our semiconductors, mainly LSIs and image sensors, have been used for various purposes including onboard products. Especially, automotive image sensors continue to evolve from the viewing stage to the sensing stage. By establishing the organization dedicated to automotive image sensor products, Sony accelerates development speed of its products and attains the high quality of automotive products at the same time. It operates the system for continuously improving the quality of automotive semiconductor products as well as streamlining of business processes for the expected automatic car driving in the future.

Figure 2-1 SSS Basic image of automotive semiconductor product quality

2.2 Philosophy about the Automotive Semiconductors Quality

We are always thinking that complying with automotive quality standards are minimal conditions for Sony automotive semiconductor products. Continuous efforts for improvement working process, will provide high quality and high reliability products to customers.

Furthermore, all people, involved in automotive products in development and production phase, aim at the goal of Zero Defect, always keeping in mind that causing failures may affect human life.

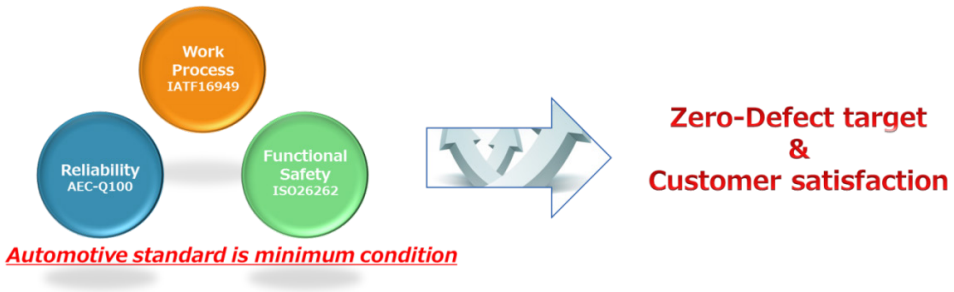


Figure 2-2 Automotive semiconductors quality philosophy image

2.3 Quality management system for automotive device (QMS)

We always monitor the latest standards so that our products can conform to the automotive semiconductors quality standards.

We have continued to ship image sensors conforming to IATF16949.

In this way, we continue to improve the quality management system allowing continuous improvement of the supply chain including sales companies and logistics with taking into consideration prevention of malfunctions and reduction of variations and waste generated in this supply chain.

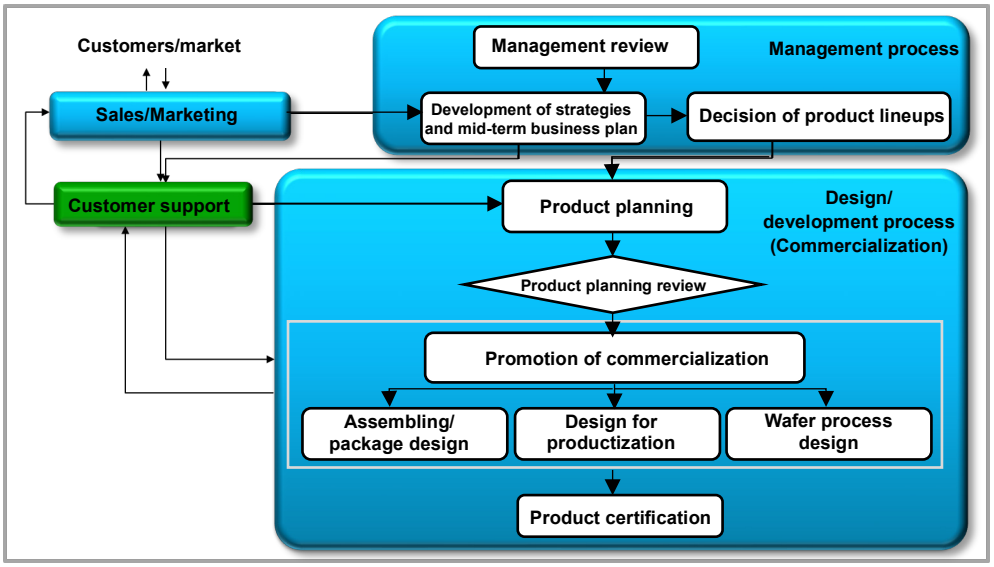


Figure 2-3 Outline of the quality management system process map

2.4 Development for Commercialization

We clarify the difference in design between automotive semiconductors and consumer products and follow the automotive product design review to promote development/ commercialization of products. In this stage, we use core tools such as Failure Mode and Effect Analysis (FMEA), Control Plan (CP) and SPC to maintain the development system from development to manufacturing. Therefore, while conforming to IATF16949, we can delegate the task from the development side to the manufacturing side via several design reviews.

Figure 2-4 Design review flow

2.5 Zero Defect

In compliance with at least AEC-Q100, we run a check and perform evaluation of wear or an initial failure so that a malfunctioning mechanism unique to an image sensor or another application can be validated.

As well as a traditional design review, we always evolve business processes such as evaluation starting from the components stage and building of functional safety into products in addition to the core tools and statistic screening in order to maintain the automotive semiconductors quality.

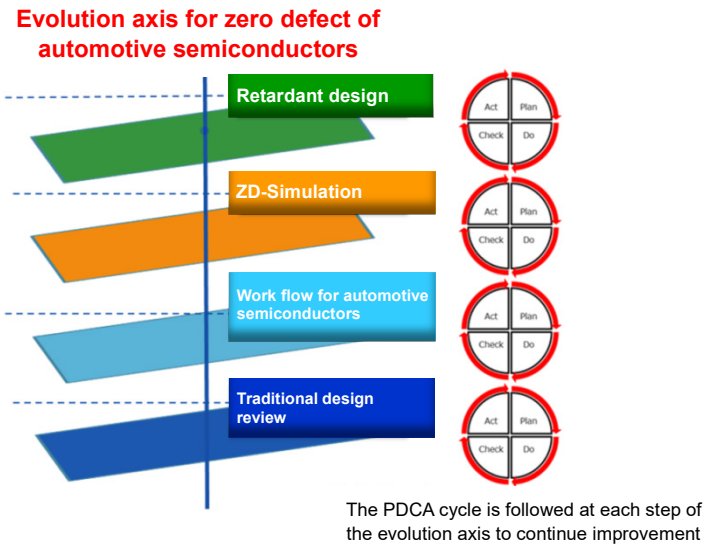


Figure 2-5 Zero defect concept image

2.6 Statistic Screening

Except for special cases, the quality reliability is closely related to the yield (and the cause of a low yield).

We incorporate screening for setting a yield limit that can be cleared by only highly reliable products detected statistically in addition to an electrical quality determination so that any products at high risk for low reliability can be prevented from being shipped.

This statistic screening method is applied to products by wafers and by lots respectively.

The method for monitoring not only a total yield value but also a yield for each of measurement categories (referred to as a BIN number) at the same is used also.

By using each method or two or more methods, we can supply highly reliable semiconductors required by automotive products.

We may also incorporate a method for forcibly rejecting a die at a location causing a malfunction very frequently by lots and/or a method for forcibly rejecting parts around a malfunctioning die.

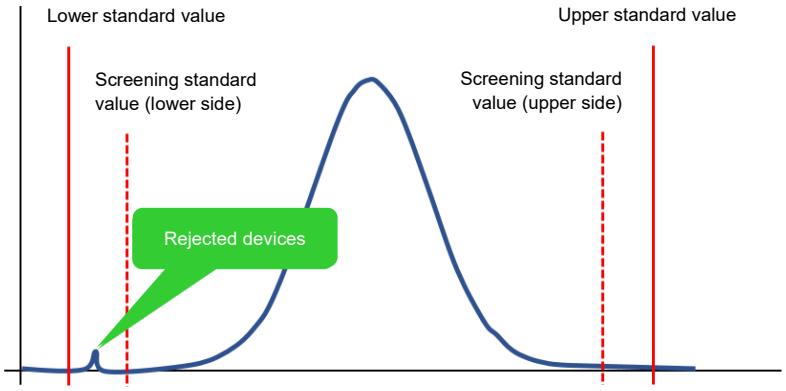


Figure 2-6 Statistic screening image (for rejecting an outlier)

2.7 Functional Safety

Products conforming to ISO26262 are designed with including a retardant system or a failure detection system. This achieves the safety of each product, and allows us to evaluate the safety. We attain the Automotive Safety Integrity Level (ASIL) required by customers' systems.

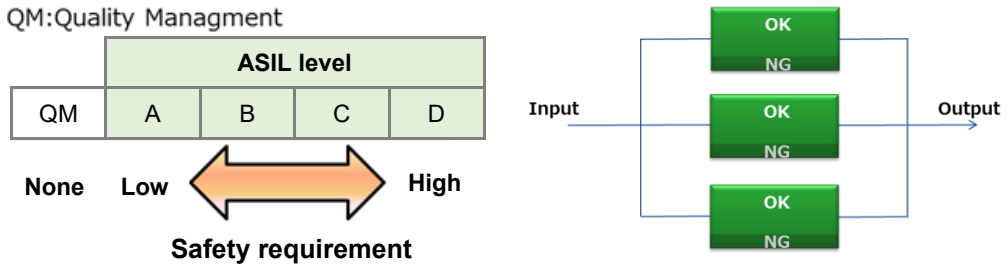


Figure2-7 ASIL level and the retardant design image

2.8 Measurement and Monitoring of the Quality

We set a KPI (key performance indicator) based on the business plan every year to review it at the in-house quality meeting as well as monitor a percent defective through a whole year. Based on the review results, we set the essential measures CTQ (Critical To Quality) for the next fiscal year to follow the PDCA (Plan-Do-Check-Act) cycle.

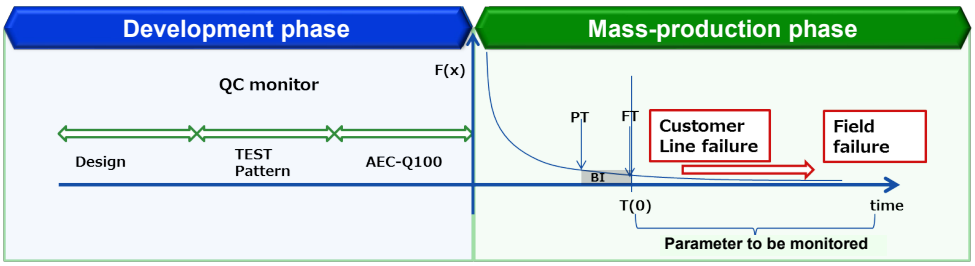


Figure2-8 Monitoring and measurement of the quality

2.9 Problem Solving

If a problem occurs at the delivery site or in the market or during development by any chance, we follow a method such as Sony six sigma method and an 8D report method to solve the problem. To solve the problem, in some cases, we may use why-why analysis, FTA (Fault Tree Analysis) or FMEA as factor analysis unique to automotive semiconductors to investigate causes and elucidate the real causes. We have already been well organized to immediately conduct product evaluation, reliability evaluation or physics analysis for determination of the real cause.

8D Method

General Description

D1. Team Approach

D2. Problem Description

D3. Containment Actions

D4. Root Cause Analysis

D5. Define of Corrective Action

D6. Implement of Corrective

D7. Action Taken to Prevent Recurrence

D8. Final Discussion

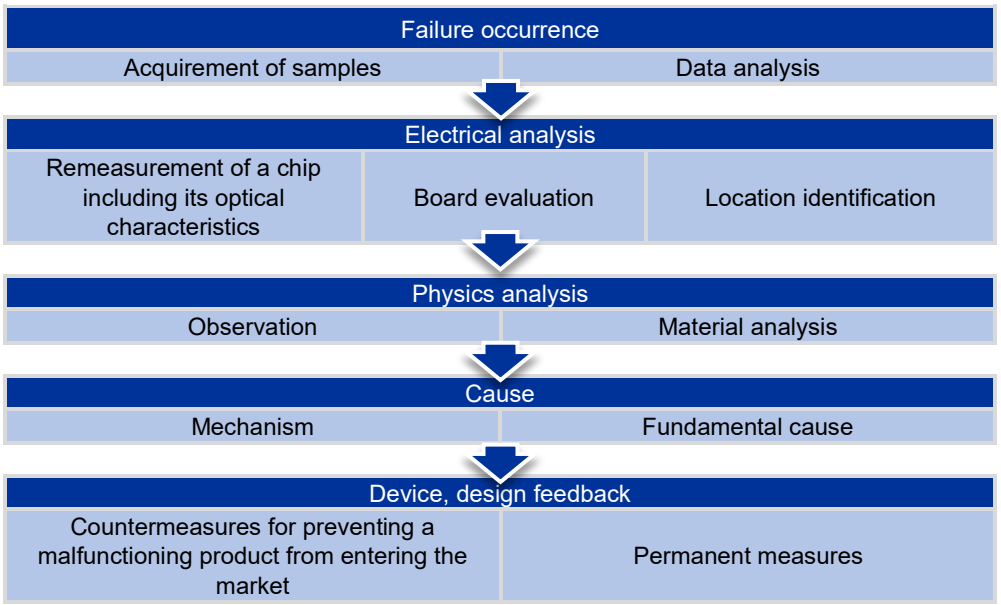


Figure2-9 Problem solving flow example

2.10 In-house Education for Automotive Semiconductors

Automotive parts such as parts for automatic driving evolve very quickly. To follow this, we monitor the latest laws and regulations for automotive parts and information on the corresponding standards to apply the new information acquired in this way to our internal education.

We increase the number of internal auditors and that of employees who can conduct a functional safety assessment to promote fostering of the automotive culture.

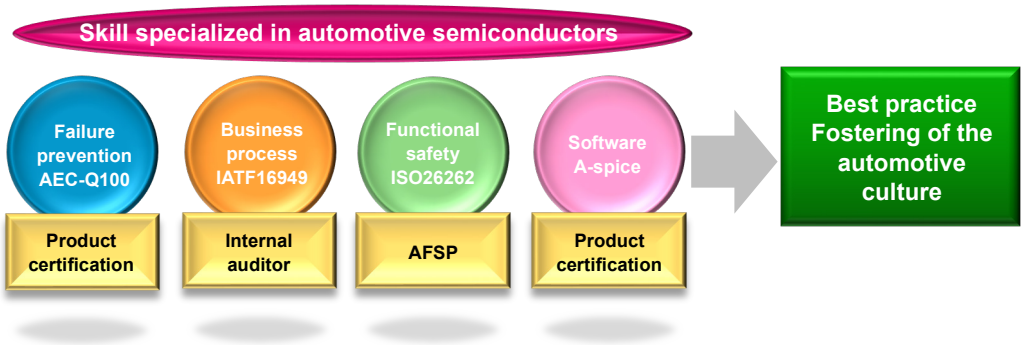
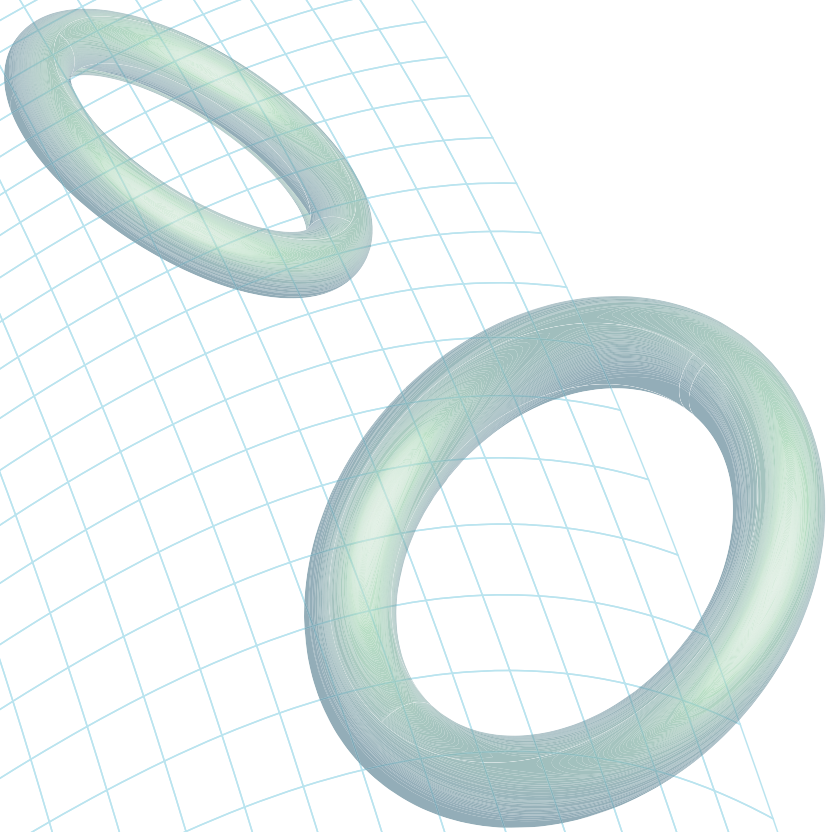


Figure2-10 Diagram of efforts for learning and growth of automotive semiconductors

Chapter 3 Software Quality



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3.1 Approach to Software Quality

3.1.1 Importance of Software

In developing a device product, the following factors increase the number of roles of software further and its development scale too:

- Enhancement of product functions
- Improvement of the hardware performance
- Restriction of the development period.

On the other hand, a failure of the embedded software directly leads to that of a product. Software of some products cannot be updated by wireless communication (OTA: On-the-Air) or similar method, and a software failure may require products to be collected or recalled. Therefore, the software quality and the software quality assurance activities are very important. The significance of software will increase further in the many areas such as IoT, M2M, in-vehicle devices and medical equipment.

3.1.2 Software Quality Assurance

Our software quality assurance is a series of activities for ensuring that software satisfies the desired quality requirements, and includes the following activities:

- Objective evaluation of the development process and work results
- Objective evaluation of the final products
- Continuous improvement of the development process

3.1.3 Software Development Life Cycle

To timely provide products that satisfy the requirements of quality which is in matching with customers' needs, we define the software development life cycle from product planning, definition of requirements, mounting, mass-production, maintenance, and then to disposal by referring to the ISO/IEC12207.

In addition to the Quality Assurance System described in Section 1.2, we conduct a design review (DR) for software.

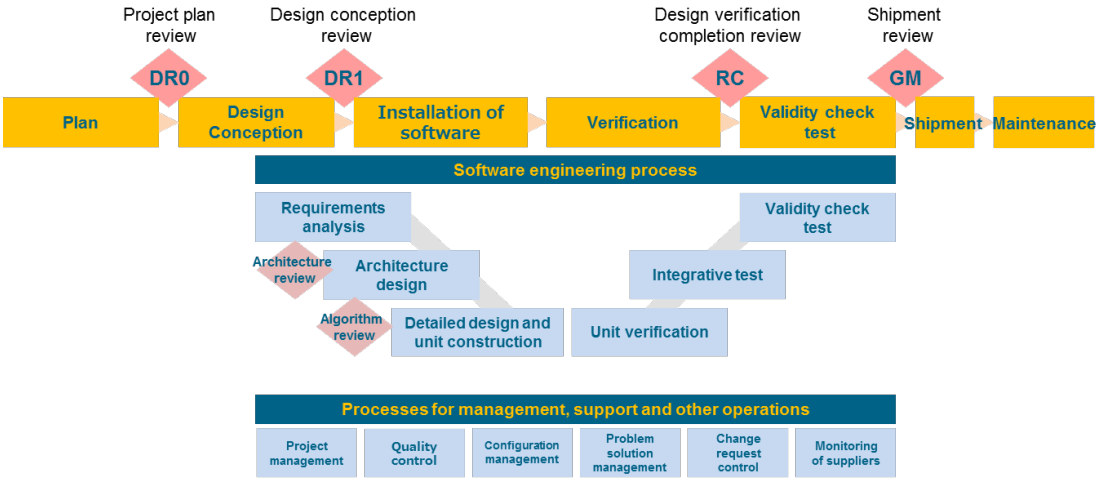


Figure 3-1 Software development life cycle

3.1.4 Software Quality Definition

ISO/IEC25000 (SQuaRE) series, which is the international standard, is used to define the versatile quality requests for a system and software.

Product Quality Model	
Functional suitability	**Reliability**
Functional completeness	Maturity
Functional correctness	Availability
Functional appropriateness	Fault tolerance
Performance efficiency	Recoverability
Time behavior	**Security**
Resource utilization	Confidentiality
Capacity	Integrity
Compatibility	Non-repudiation
Co-existence	Accountability
Interoperability	Authenticity
Usability	**Maintainability**
Appropriateness recognizability	Modularity
Learnability	Reusability
Operability	Analysability
User error protection	Modifiability
User interface aesthetics	Testability
Accessibility	**Portability**
	Adaptability
	Installability
	Replaceability

Quality in use
Effectiveness
Efficiency
Satisfaction
Usefulness
Trust
Pleasure
Comfort
Freedom from risk
Economic risk mitigation
Health and safety risk mitigation
Environmental risk mitigation
Context coverage
Context completeness
Flexibility

Figure 3-2 System and software quality models [ISO/IEC 25010:2011 Systems and software engineering – Systems and software Quality Requirements and Evaluation (SQuaRE)]

3.1.5 Detection of a Defect

The measures such as the following front loading measures are taken in order to detect a defect in the early stage, take a countermeasure for it, and then improve the software quality.

- Static Analysis

  By using a static analysis tool to analyze the source codes in the software coding and single substance unit test stage, a defect(s) and a problem(s) of the detailed design are found directly from the source codes.

- Review

  A peer review is executed during development of work results (specifications, design documents and source codes) to identify a defect(s) to be eliminated before the software is operated.

- Continuous Integration

  Building and test are conducted regularly by using a tool such as Jenkins in the stage at which building can be conducted. This not only detects inconsistency of the interface in the early stage but also executes the static analysis and runs a regression test to find a failure in the early stage, and then improve the software quality.

- Simulation

  Hardware (an actual machine) and the embedded software are developed at the same time in several cases. Logical simulation that makes use of the FPGA or EDA tool is used to perform timing verification or similar check before testing the actual machine.

- Scrum development method

  We have started to use the Agile scrum development method. The following effects are expected: reduction of a return risk caused by a perception gap of requirements and a risk of change of the requirements, and reduction of returned products due to recognition of a risk in the early stage.

3.1.6 Approach to Fault Prevention

Not only tests but also the following fault prevention methods are conducted to improve the quality and the development efficiency.

- Failure Mode and Effect Analysis (FMEA)

- Clarifying problems and taking measures for them

  Persons involved gather to identify a problem based on the causes of failures already occurred and the differences from the original software.

- Process model

  Improvement of the process quality leads to improvement of the process output and work results qualities. Therefore, we establish a process by referring to the CMMI or SPICE practices. Automotive-SPICE is installed especially in order to develop software for in-vehicle devices.

3.1.7 Defect Analysis

A defect is analyzed with using a tool such as Orthogonal Defect Classification (ODC) in the development stage. The quality obtained at this point is checked, and then fed back to the test plan or process improvement.

When a defect is found in the maintenance stage or when a critical defect is found even in the development stage, analysis such as the Fault Tree Analysis (FTA) and the why-why analysis is executed to identify the true cause, and then lead to the activities for preventing the defect from reoccurring.

3.1.8 Use of Open Source Software (OSS)

In response to request for development of software such as diversification of functions of a product, increase in the software development scale and complexity, and shortening of the release cycle, use of the high quality Open Source Software (OSS) is one of the most effective solutions for cost reduction and shortening of the development period. To understand the OSS license correctly and use it appropriately, we have established the mechanism for objective inspections and consultation incorporated into the software development life cycle.

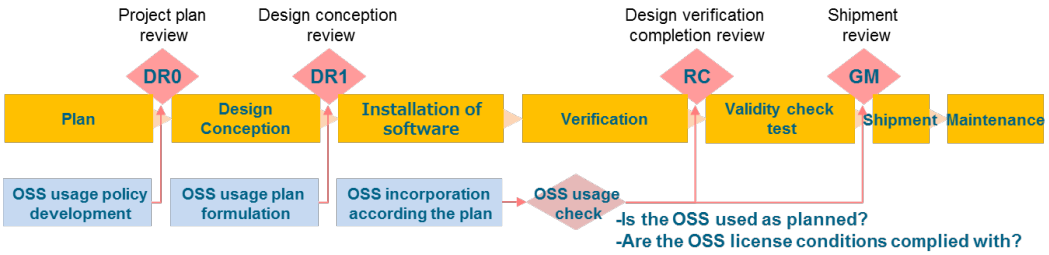


Figure 3-3 Usage of the open source software (OSS)

3.2 Approach to the Security of Products

3.2.1 Importance of the Security of Products

Threat to security of home appliances such as a TV and a digital camera and built-in products such as an in-vehicle product has spread recently, and a case of threat to a semiconductor product such as leakage of an encryption key has been reported also. Under this condition, not only as our company but also as the Sony group, we recognize the importance of the security of products and take the appropriate countermeasures against it.

3.2.2 Product Security Development Life Cycle

As the product security countermeasure, we define the security development life cycle shown in Figure 3-4 to introduce it. We take practices for improving the security quality from the planning stage to disposal stage of a product. This reduces the product security quality problem (security incident) occurrence rate and its effect, and allows us to take an immediate and appropriate countermeasure against an incident that happens to occur after shipment if by any chance.

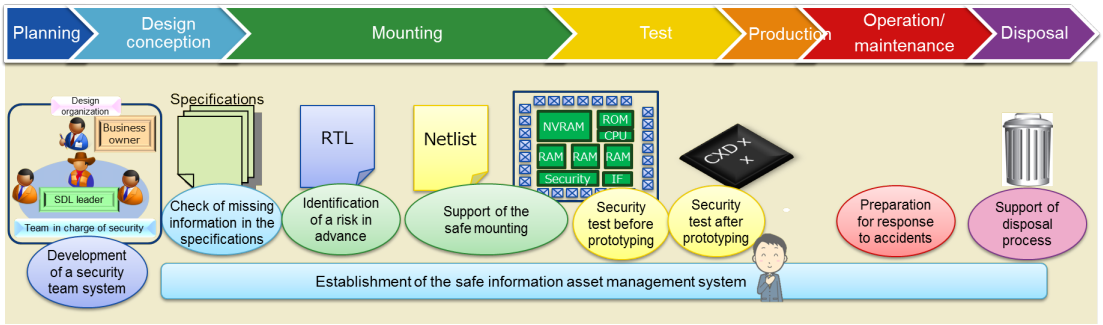
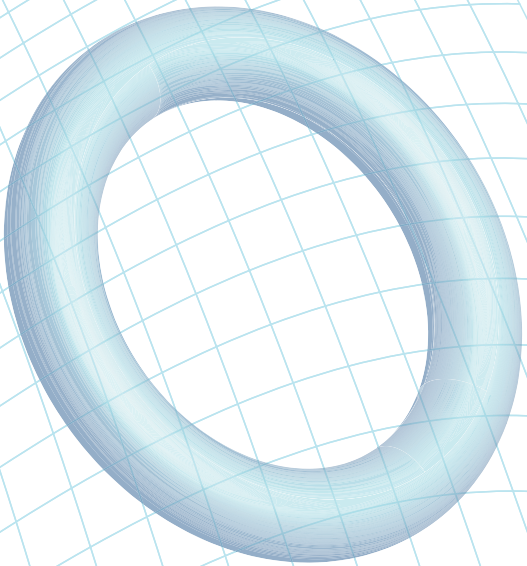


Figure 3-4 Product security development life cycle

Chapter 4 Reliability of Semiconductor Devices



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4.1 Fundamental Knowledge on Semiconductor Reliability

With recent advances in systematization, functionality and performance of equipment, social impact and damages produced by failures have increased, and high reliability has come to be required for equipment. This means that further higher reliability is required for each component configuring the equipment.

Numerous semiconductors are used in a single piece of equipment, and these semiconductors undertake the main functions of the equipment in many cases, so high reliability of semiconductors is extremely important. Semiconductors themselves have also become more miniaturized and highly integrated, and have required larger-scale circuit configurations. Since functions and performance of semiconductors have reached to the further higher level and large-scale integrated circuits have tended to make up semiconductors as a system too, ensuring of semiconductor reliability has become more important than ever before.

The reliability scale, distribution functions, temporal transition of the failure rates, and failure regions all of which are needed to discuss semiconductor reliability are described below.

4.1.1 Scale for Representing the Reliability

JISZ 8115 “Glossary of terms used in dependability (reliability)” defines reliability as “the property of an item which enables it to fulfill its required functions during the prescribed time period under the given conditions.” Therefore, reliability includes the concept of time, and the scale of reliability is a function of time.

(1) Reliability Function (Degree of reliability): R(t)

The degree of reliability indicates the probability for functioning correctly without malfunctioning until the time “t.”

When n samples are used under the same conditions, and the number of failures occurring until the time “t” has elapsed is expressed as “r(t),” the degree of reliability R(t) is expressed by the following expression.

$$R(t) = \frac{n - r(t)}{n} \qquad \cdots \text{ Expression 4.1.1}$$

(2) Failure Distribution Function (Degree of unreliability): F(t)

The degree of unreliability indicates the probability of malfunctioning until the time “t” has elapsed and is expressed by the following expression.

$$F(t) = \frac{r(t)}{n} \qquad \cdots \text{ Expression 4.1.2}$$

In addition, the following relation is established between the degree of unreliability F(t) and the degree of reliability R(t).

$$R(t) + F(t) = 1 \qquad \cdots \text{ Expression 4.1.3}$$

As shown in Figure 4-1, R(t) decreases from “1” over time, while conversely F(t) increases from 0 toward 1 over time. Note that the distribution functions described below are used as the failure distribution functions of semiconductor devices.

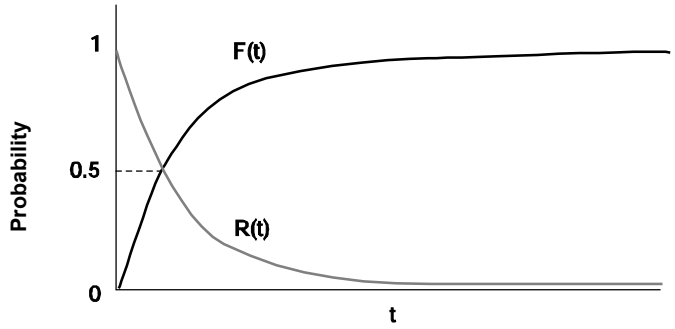

Figure 4-1 Relation between F(t) and R(t)

(3) Failure Density Function: f(t)

The failure density function represents the probability of malfunctioning per unit time when time “t” has elapsed.

$$f(t) = \frac{dF(t)}{dt} = -\frac{dR(t)}{dt} \qquad \cdots \text{ Expression 4.1.4}$$

(4) Failure Rate Function: λ(t)

The failure rate function represents the rate at which samples that have not yet malfunctioned malfunction in the next unit time when time “t” has elapsed.

$$\lambda(t) = \frac{f(t)}{1 - F(t)} = \frac{f(t)}{R(t)} \qquad \cdots \text{ Expression 4.1.5}$$

The failure rate function is also called the instantaneous failure rate, and it is calculated from the failure distribution function F(t) with using Expressions 4.1.4 and 4.1.5. Failure In Time (FIT: number of failures per billion (10^9) total operating hours) is generally used as the unit for semiconductor devices.

Note that when the F(t) of the subject product is not known, the average failure rate obtained by the following expression is used.

Average failure rate ≡ Total number of failures that occurred during the period / Total operating time during the period ··· Expression 4.1.6

[Supplementary information]

In addition to the failure rate defined above, the cumulative failure rate to be applied after a set on which a semiconductor device is mounted operates for the specified time in the market is sometimes used in the early “infant mortality” failures region described below. Unless otherwise requested by any customer, we also use the cumulative failure rate after one year as the early failure rate.

In addition, after the early failures region, many semiconductor devices do not reach a wear-out failure (real failure) state in the actual operating environment, and the failure rate shows the constant value of the accidental failures region. Since this value is equal to that obtained by Expression 4.1.6, the average failure rate can be said to be the failure rate after the early failures region practically.

(5) Mean Time To Failure: MTTF

The Mean Time To Failure (MTTF) of an item such as a semiconductor device that is not subject to repair or maintenance is expressed by the following expression.

$$MTTF = \int_0^\infty tf(t)dt \qquad \cdots \text{ Expression 4.1.7}$$

4.1.2 Distributions Used in Reliability Analysis

Typical distribution functions used to analyze reliability data of semiconductor devices are described below.

(1) Normal distribution

The normal distribution is one of typical continuous distributions used for quality control. It is said that in reliability analysis, the normal distribution is applied to wear-out failures that occur intensively at some point.

The failure density function f(t) and the distribution function F(t) are expressed by the following expressions.

$$f(t) = \frac{1}{\sqrt{2\pi}\sigma}\exp\left\{-\frac{(t-\mu)^2}{2\sigma^2}\right\} \quad (-\infty < t < \infty) \qquad \cdots \text{ Expression 4.1.8}$$

$$F(t) = \frac{1}{\sqrt{2\pi}\sigma}\int_{-\infty}^{t}\exp\left\{-\frac{(x-\mu)^2}{2\sigma^2}\right\}dx \quad (-\infty < t < \infty) \qquad \cdots \text{ Expression 4.1.9}$$

This distribution is given by the parameter μ indicating a mean value and the parameter σ indicating the dispersion (variance).

As shown in Figure 4-2 below, the normal distribution has a symmetrical bell shape centering on μ, and the value t is contained at the probability of 68.26 % in the range ±σ on both sides of μ, 95.44 % in the range of ±2σ on both sides of μ and 99.7 % in the range of ±3σ on both sides of μ respectively.

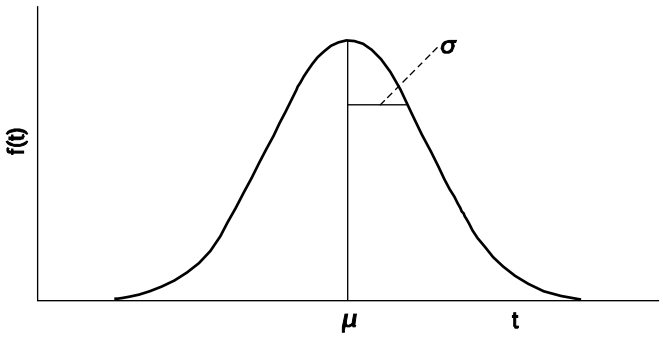

Figure 4-2 Normal distribution

(2) Exponential distribution

The exponential distribution is applied to the life distribution (failure distribution function) in the accidental failures region where the failure rate λ becomes constant over time, and the probability density function f(t) and the Cumulative distribution function F(t) are expressed by the following expressions respectively. This distribution is equivalent to the Weibull distribution described below when the shape parameter m = 1.

$$f(t) = \lambda \ \ 〖exp〗 \ ^((-\lambda t)) \quad \cdots \text{ Expression 4.1.10}$$

$$F(t) = 1 - \ \ 〖exp〗 \ ^((-\lambda t)) \quad \cdots \text{ Expression 4.1.11}$$

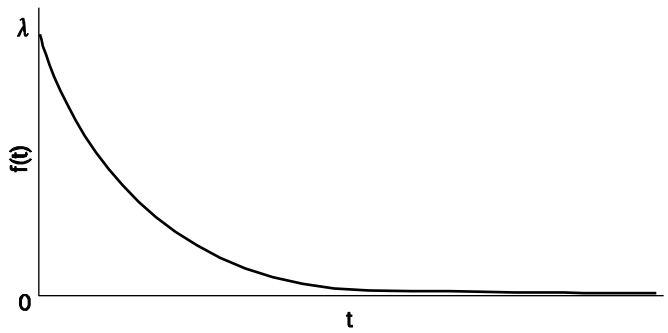

Figure 4-3 Exponential distribution

Note that as shown in the following expression, the MTTF is given from t_0, which is an inverse number of the failure rate λ.

$$1/\lambda = t_0 = MTTF \quad \cdots \text{ Expression 4.1.12}$$

(3) Log-normal distribution

The log-normal distribution is a distribution function where ln t, which takes the logarithm of the life time "t," follows the normal distribution described above.

The probability density function f(t) and the distribution function F(t) are expressed by the following expressions.

$$f(t) = \frac{1}{\sqrt{2\pi}\sigma t}\exp\left\{-\frac{1}{2}\left(\frac{\ln t - \mu}{\sigma}\right)^2\right\} \quad (0 < t < \infty) \quad \cdots \text{ Expression 4.1.13}$$

$$F(t) = \frac{1}{\sqrt{2\pi}\sigma}\int_0^t \frac{1}{x}\exp\left\{-\frac{1}{2}\left(\frac{\ln x - \mu}{\sigma}\right)^2\right\}dx \quad \cdots \text{ Expression 4.1.14}$$

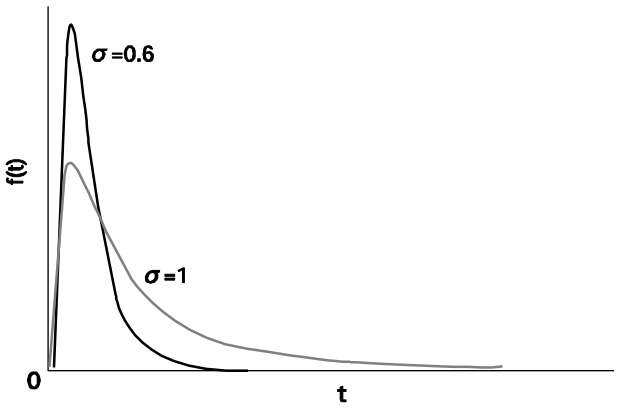

Figure 4-4 Log-normal distribution

As for the reliability of a semiconductor device, the electromigration life is generally known to follow this log-normal distribution.

(4) Weibull distribution

The Weibull distribution is a weakest link model proposed by ***W. Weibull*** (Sweden) in 1939 as breaking strength distribution of a machine. This model is said to have been applied to analyze the life of vacuum tubes by ***J. H. K. Kao*** in 1955, and has often been used since then for model life distributions in analysis of semiconductor device reliability.

The probability density function f(t) and the distribution function F(t) are expressed by the following expressions.

$$f(t) = \frac{m}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{m-1} \exp\left\{-\left(\frac{t-\gamma}{\eta}\right)^{m}\right\} \quad \cdots \text{ Expression 4.1.15}$$

$$F(t) = 1 - \exp\left\{-\left(\frac{t-\gamma}{\eta}\right)^{m}\right\} \quad \cdots \text{ Expression 4.1.16}$$

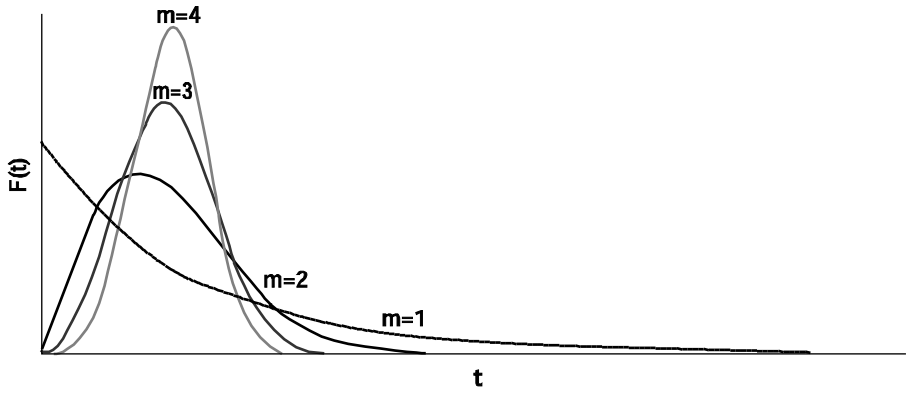

Figure 4-5 Weibull distribution

Here, m is called a shape parameter, η a scale parameter (characteristics life), and γ a position parameter.

In addition, assuming $t_0 = \eta^m$, the failure rate λ (t) is expressed by the following expression.

$$\lambda(t) = \frac{m}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{m-1} = \frac{m}{t_0}(t-\gamma)^{m-1} \qquad \cdots \text{ Expression 4.1.17}$$

The following information on the malfunction pattern can be obtained from the value of the shape parameter m.

When 0 < m < 1: Early failure pattern where the failure rate decreases over time (decreasing failure rate: DFR)

When m = 1: Accidental failure pattern where the failure rate is constant (matches the exponential distribution) (constant failure rate: CFR)

When m > 1: Wear-out failure pattern where the failure rate increases over time (increasing failure rate: IFR)

4.1.3 Semiconductor Device Failure Pattern

4.1.3.1 Semiconductor Device Failure Regions

As shown in Figure 4-6, like general electronic equipment, the failures region of semiconductor devices is classified into the three types: early, accidental and wear-out failure regions, and temporal transition of the failure rate describes a curve called a bathtub curve.

This curve consists of the early failure rate which decreases monotonously over time, the accidental failure rate which shows a constant value, and the wear-out failure rate which increases monotonously over time. However, in case of semiconductor devices, only phenomena like a soft error whose occurrence rate is extremely low are observed in the accidental failure period as described below. The failure rate in the accidental failures region (the height of the bottom of the bathtub) is supposed to show the remaining failures that occurs after the early failure rate converges.

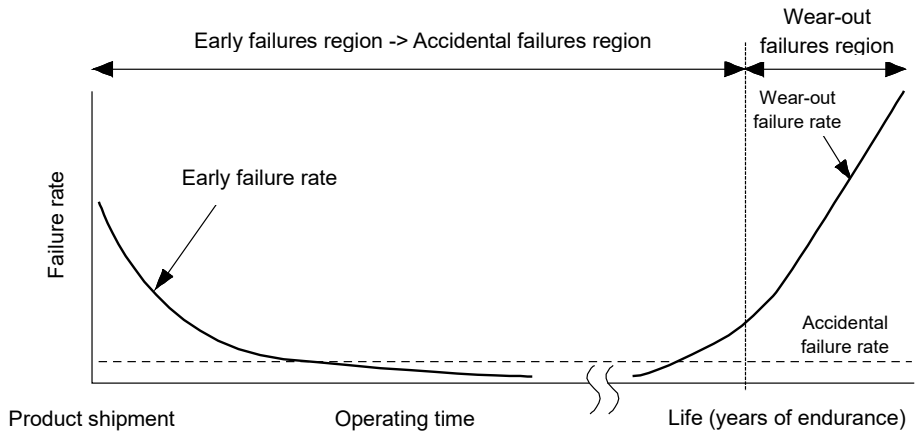

Figure 4-6 Change in the failure rate of a semiconductor device over time

4.1.3.2 Early Failures

The failure rate in the early failure period is called EFR (early failure rate), and the failure rate tends to decrease over time. Many of semiconductor device early failures are caused by defects that were built into devices mainly during the wafer process. The most common causes of these defects are dust stuck to wafers during the wafer process and crystal defects of the gate oxide film or the silicon substrate and so on. Most devices containing defects derived from the manufacturing process are recorded during the manufacturing process, and then eliminated as defective products during the final sorting process. However, devices having relatively insignificant defects may be shipped as accepted products because they show the similar electrical characteristics with those of an accepted product when the final measurement is conducted. Since these types of devices having such an insignificant defect malfunction in a short time, they can be eliminated when high stress (such as voltage and temperature) is applied to them. The screening to eliminate weak devices with inherent initial defects is called “wafer level burn-in” in the wafer status and “burn-in” in the package status.

Recent devices have hardly shown any early failure during validation of the development stage.

This is because the technology for preventing contamination or defects has evolved in the latest automated manufacturing line, the precision of the in-line defect inspection has improved, and systems for visualizing all defects to associate them with electrical characteristics have improved drastically. At the same time, advances of the automatic design technology (simulation) have also raised the robustness to defects and this allows high quality robust over variations to be obtained from the development stage. As for screening of an early failure, conducting of a stress test in a wafer state, therefore, secures sufficiently high quality in many cases.

The overview of burn-in as a method for screening of early failures is described below.

(1) Deriving of a failure distribution function in an early failure period

In order to determine the burn-in conditions for securely eliminating devices having early (initial) defects, it is necessary to obtain a failure distribution function in an early failure period.

To obtain this function, highly accelerated life tests are performed in a short time with using numerous samples including devices having initial defects (normally several thousand to ten thousand samples). The obtained failure time data is then plotted on Weibull probability paper and the failure distribution function is estimated from the resulting regression line.

Figure 4-7 shows an example of this process. The shape parameter m and the characteristic life η that determine the Weibull distribution in the following expression can be obtained from the regression line.

$$F(t) = 1 - exp\{-(t/\eta)\hat{}m\}$$ ･･･ Expression 4.1.18

This method for obtaining the failure distribution function is referred to as “burn-in study.”

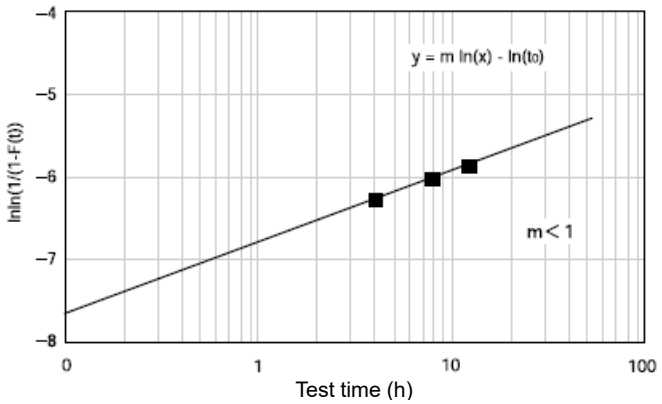

Figure 4-7 Weibull plot of the burn-in study

Note: Weibull probability paper is scaled to display linear regression of the failure time when the failure time follows a Weibull distribution.

(2) Determining the burn-in conditions

The screening (burn-in) conditions required to reduce the early failure rate (Note 1) after shipment to the target value can be determined with using the failure distribution function F(t) obtained from the burn-in study.

When the burn-in time is set as t_0 and the acceleration coefficient between the burn-in conditions and the market environment as A_F, the cumulative early failure probability that can be eliminated by burn-in is given as $F(A_F \cdot t_0)$, and the new accumulated early failure probability F(t) by time t after burn-in is performed can be obtained by the following expression.

$$F(t) = F(A_F \cdot t_0 + t) - F(A_F \cdot t_0) \qquad \cdots \text{ Expression 4.1.19}$$

This relation can be expressed in a graph as shown in Figure 4-8.

The burn-in conditions are selected according to a combination of the acceleration conditions and time that will reduce this value to the target early failure rate or lower. Normally, the frequency of initial defects that cause early failures to occur becomes the highest in the initial stages of process development, and then decreases as the process is improved and the process master level becomes higher. The early failure rate decreases in proportion to the frequency of these initial defects, so the burn-in time has to be reviewed in accordance with improvement of the process.

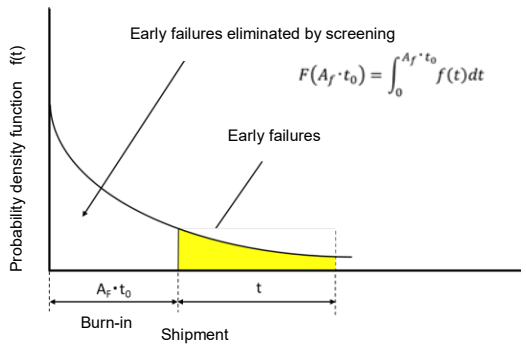

Figure 4-8 Screening of the early failures by burn-in

Note 1: The early failure rate described in this section is not the instantaneous failure rate but the cumulative failure probability within a specified period.
See “Supplementary information” of Section 4.1.1 “Scale for Representing the Reliability.”

4.1.3.3 Accidental Failures

After devices containing early failures are eliminated to a certain degree, any failure does not occur for a long time from the early failure period to the end of the durable service life: this is a stable period of devices. In this region, the failure distribution is close to an exponential distribution, and this period is referred to as the accidental failure period. Since the semiconductor device failure rate during this accidental failure period is an extremely small value in comparison with the early failure rate shown immediately after shipment, it is hardly observed even in mass-produced products. From the point of view of semiconductor devices malfunctioning mechanism, any failures cannot be clearly defined as accidental failures either, and memory soft errors and other phenomena caused by high-energy particles such as radiation generated depending on the use environment are sometimes classified as accidentally occurring failure mechanisms.

When the semiconductor device failure rate is predicted, failures occurring sporadically after a certain long time passes since the start of operation and those whose cause cannot be determined are regarded as accidental failures in some cases. However, most of these failures are thought to be caused because devices having relatively insignificant initial defects (such as dust and crystal defects) malfunction after a long time, and should be originally positioned at an early failure rate attenuation curve. As an index, a mean failure rate is estimated with assuming the exponential distribution in some cases. Although this rate cannot be strictly estimated from the results of tests performed with a few samples such as reliability tests, it is treated as an estimated value (a guide) larger than the actual value. Failure in Time (FIT) is used as a unit.

There are also phenomena such as electrostatic breakdown, overvoltage (surge) breakdown (EOS) and latch-up that occur in the accidental period according to the use conditions. Since these phenomena are all the mechanism affected by an external factor, for example, application of excessive stress over the absolute maximum rating of a device to the device, these are classified as breakdowns instead of failures, and are not included in the accidental failures.

4.1.3.4 Wear-out Failures

Wear-out failures are derived from the durability of materials comprising semiconductor devices or from elements such as transistors, wiring and oxide films, and they are indexes for determining the device life (years of endurance). In the wear-out failures region, the failure rate increases with the lapse of time until finally all devices malfunction or lead to property defects.

The main wear-out failure mechanisms of semiconductor devices are described below.

- Electro-migration
- Hot carrier-induced characteristics fluctuation
- Bias Temperature Instability (BTI) of characteristics
- Time-dependent dielectric breakdown (TDDB)
- Laser diode luminance degradation

Basically, the reliability of semiconductor devices is supposed to be developed and validated with using Test Element Groups (TEG) for each component of the devices. The validated huge amount of data is reflected in the design tools, and then products are designed so that they can reach the reliability goal. Unreasonable usage of a product and deviation from the designing rules are checked with the design tools to prevent a wear-out failure from occurring under the actual use environment and secure the long-term reliability. Therefore, wear-out failures hardly occur in the reliability test that is performed as verification in the semiconductor product development stage.

(1) Life estimation method

The lifetime of a device in the market environment can be computed using the failure data from the TEG evaluation and the reliability test. The value can be obtained by linearly regressing the cumulative failure probability at the lapse of time by the Weibull probability paper or the log normal random probability paper to calculate the time to reach the reference cumulative failure probability (or stress) to be used as a reference value and the acceleration magnification of the acceleration test condition (Figure 4-9).

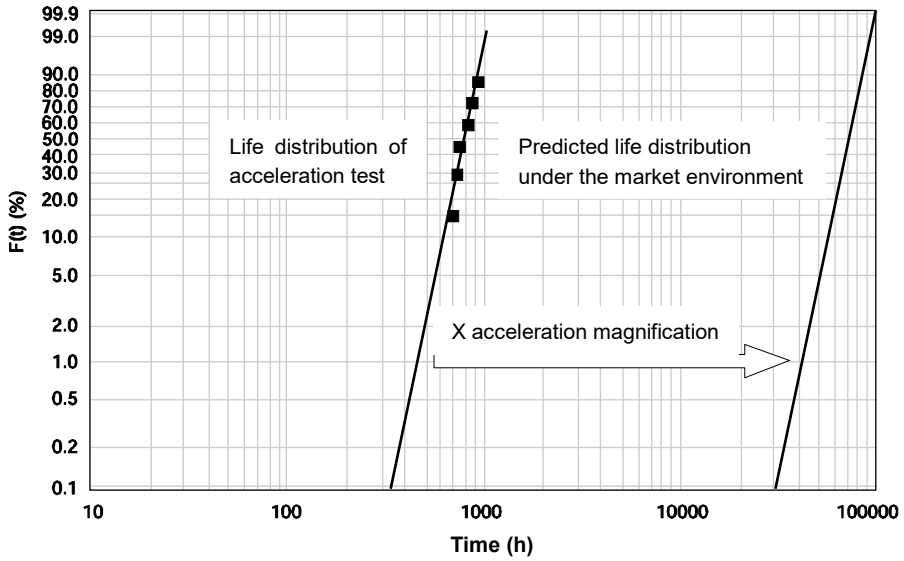

Figure 4-9 Life estimation method with using Weibull probability paper

4.2 Semiconductor Reliability Verification

4.2.1 Basic Concept of Reliability Verification

We perform reliability verification that takes into consideration semiconductor device failure modes (see Figure 4-10) in each stage from process development to mass production.

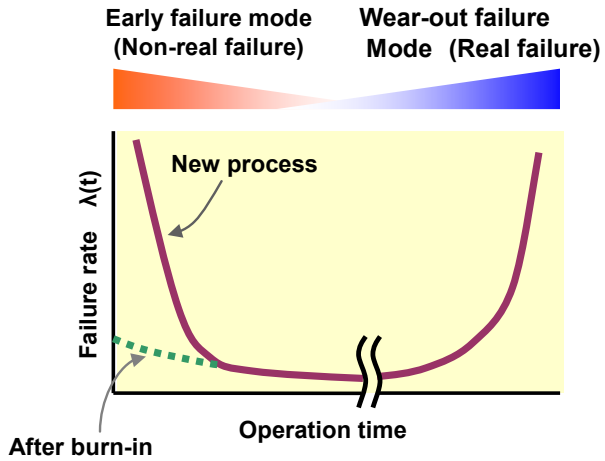

Figure 4-10 Semiconductor device failure rate curve

4.2.1.1 Semiconductor Reliability Verification in the Development Stage

The failure period generated due to wear-out failures (that is, real failures) of semiconductor devices, which means the life of the devices, is determined by the failure mechanisms of the process elements described in 4.2.2.

Reliability is evaluated in the process development stage with using test element groups (TEG) appropriate for verifying these failure mechanisms to check that the prescribed reliability is satisfied.

4.2.1.2 Reliability Verification in the Prototyping Stage

(1) Reliability verification for wear-out failures (real failures)

Reliability is evaluated over long time with using small quantities of prototypes to verify that any wear-out failure does not occur in the assumed operating environments during the assumed use period. (See Table 4-1.)

(2) Reliability verification for early failures (non-real failures)

The failure rate of semiconductor devices tends to be high at the start of operation, and then tends to decrease monotonously over time.

This is because a certain percentage of semiconductor devices that have a manufacturing defect such as dust malfunction. Since this tendency is more noticeable in new processes, burn-in studies are performed to verify the early failure rate when the corresponding production is introduced.

When the prescribed failure rate is not satisfied, screening methods such as burn-in are used to remove semiconductor devices having manufacturing defects.

We continuously try to execute activities for stabilizing and improving processes, and reduce the number of semiconductor devices having manufacturing defects so that the prescribed early failure rate can be satisfied without performing burn-in.

4.2.1.3 Reliability Verification in the Mass Production Stage

Periodically mass-produced products are sampled* and their reliability is evaluated at the product level equivalent with (1) above to check that the wear-out failure reliability level attained at the development stage is continuously maintained after mass-production too.

* Samples are taken from each product family with considering combinations of a wafer process, an assembly process, a manufacturing site, and other factors.

Table 4-1 shows our typical reliability test items of LSI products.

Table 4-1 Our typical reliability test items (example)

Test name	Abbreviation	Test conditions
High Temperature Operating Life	HTOL	Tj ≧ 125 °C Vop_max 1000 h
Low Temperature Operating Life	LTOL	Ta = -55 °C Vop_max 1000 h
Temperature Humidity Bias	THB	Ta = 85°C85%RH Vop_max On/Off 1000 h
High Temperature Storage	HTS	Ta=150 °C 1000 h
Temperature Cycling	TC	Ts = -55~125 °C 700 cyc Ts = -40~125 °C 850 cyc Ts = -65~150 °C 500 cyc
Moisture Sensitivity Level	MSL	Level-3 (Standard rank) (J-STD-020)
HBM Electrostatic Discharge Human Body Model	ESD HBM	C = 100 pF, R = 1500 Ω (JS-001-2014)
CDM Electrostatic Discharge Charged Device Model	ESD CDM	Device charged model (JESD22-C101)
Latch-Up Trigger Pulse Current Injection Method	LU I-Test	Trigger pulse current injection method (JESD78)
Latch-Up Supply Overvoltage Method	LU V-Test	Power supply overvoltage method; Ta = 25, 125 °C (JESD78)
Burn-In Study (Early Life Failure Rate)	BIS (ELFR)	Tj ≧ 125 °C, Vop_max

4.2.2 Reliability in the Development and Design Stages

Semiconductor devices have failure mechanisms unique to semiconductors, and resolving these problems in the process development stage is an important element for securing reliability. Product reliability can be secured stably by verifying the required reliability in the development stage of each process element and reflecting these results in the design rules.

Table 4-2 shows the typical failure mechanisms that can present problems in the process development stage. As processes become more miniaturized, the stress applied to transistors and wiring such as internal electric fields, current densities, and wiring stress increases. On the other hand, since the operation margin deteriorates due to the higher circuit speeds and increased parasitic impedance (wiring resistance, parasitic capacitance), and this leads to a major issue in securing reliability with respect to transistor characteristics fluctuation.

Typical semiconductor device failure mechanisms that can present problems in the process development and design stages are described below.

Table 4-2 Typical failure mechanism in the process development stage

Process element	Failure mechanism	Failure mode and cause
Gate insulating film	Oxide film time-dependent dielectric breakdown (TDDB)	Dielectric breakdown of the gate insulating film. This is a phenomenon: bias applied to a gate electrode for a long time produces defects in the gate insulating film, and then micro leak current increases or dielectric breakdown occurs.
Transistor	Hot carrier (HCI)	Transistor characteristics fluctuation caused by hot carriers trapped by a gate insulation film. This is a phenomenon: high-energy electrons and positive holes generated due to ionization collisions of electrons accelerated in high electric fields are trapped in the oxide film, and this causes the transistor characteristics to fluctuate.
	NBTI (slow trap)	PMOS transistor characteristics fluctuation caused by application of a gate negative bias (NBT). This is also called a slow trap phenomenon, and application of a bias at high temperature raises the interface level and increases positive fixed charge, and then this causes the transistor characteristics to fluctuate.
Memory device	Soft error	Memory data rewrite error caused by high-energy cosmic ray particles (such as neutron rays and proton ray), α rays, and so on. This is a temporary data error phenomenon that occurs mainly in a DRAM or an SRAM.
	Retention/disturb	Non-volatile memory data loss. This is a phenomenon: long-term storage or operating environment stress (read/write electric field, temperature, stress) causes the captured charge in flash memory to be lost, and then inverted.
Wiring	Electromigration	Increase of wiring resistance and disconnection caused by voids generated in the wiring. This is a phenomenon: physical collisions between electrons and metal atoms cause the metal atoms to move, and then voids occur.
	Stress migration	Metal creep phenomenon caused by stress applied to the wiring. Voids grow in the wiring and connection parts (via holes), and they cause open failures to occur. In copper wires, stress applied to the wiring causes defects in the copper wires (atom vacancy) to generate a creep phenomenon and then make voids grow.
Low-k interlayer films	TDDB between wires	Short-circuit caused by dielectric breakdown between copper wires. This is a phenomenon: dielectric breakdown via the CMP interface of an interlayer insulation film that uses low-k materials causes a short-circuit between wires.

4.2.2.1 Time-dependent Dielectric Breakdown (TDDB) of a Gate Insulation Film

A MOS FET gate insulation film has a failure mechanism that causes the insulation film to degrade and then be broken when an electric field whose voltage is the withstand voltage or less is applied to it for a long time. This breakdown of the insulation film over time is called time-dependent dielectric breakdown (TDDB). The TDDB life of gate insulation film is one of the most important failure mechanisms that determine the long-term reliability of a MOS-type semiconductor device. The TDDB life is said to be a factor that determines the micronizing level limit of the gate insulation film thickness, and the gate insulation film thickness of a system LSI is also sometimes determined according to the TDDB life corresponding to the logic circuit supply voltage.

(1) Lifetime distribution of gate insulation film

Time-dependent insulation film breakdown phenomena can generally be divided into an initial failure area and a real-life area. Figure 4-11 shows the TDDB measurement data of a gate oxide film (SiO_2) plotted with using a Weibull distribution function. The initial failure area and the real-life area can be classified by differences of the shape parameters (inclination of the graph) of the Weibull distribution. Insulation films distributed in the initial failure area whose TDDB life is short are oxide films containing defects that may malfunction in a short time in the market. It is important to suppress the defect occurrence rate in order to lower the early failure rate.

On the other hand, the real failure area indicates the original life of gate insulation film that does not contain any major defects, and it is an index required for assuring long-term reliability. The real life at the actual operating voltage can be predicted with using an electric field acceleration model based on the evaluation results of TDDB accelerated according to the high electric field stress conditions. An electric field acceleration model such as E-model ($\tau \propto \exp(E)$) and Power-law model ($\tau \propto E^{-n}$) is used depending on the film thickness and film quality. (See Figure 4-12.)

(2) Gate insulation film breakdown mechanism

Gate insulation film contains a large number of micro defects and impurities that are generated in the wafer process, and micro leak currents flow via these defects even in the state where the applied electric field (power supply voltage) is less than the real withstand voltage. These leak currents generate new defects in the insulation film over time, and accumulation of these defects leads to insulation film breakdown.

The percolation model is a typical failure mechanism for TDDB breakdown of thin gate insulation film. In this failure model, tunneling current flowing as a result of application of an electric field in addition to defects existing in the gate insulation film initially generates a new defect in the thickness direction continuously, and this leads to insulation breakdown. (See Figure 4-13.)

The thinner gate insulation film becomes, the fewer defects may generate continuous defects causing insulation breakdown. The TDDB life variation, therefore, increases. In addition, data written in flash memory is also lost (phenomenon of retention) due to micro leak currents prior to breakdown.

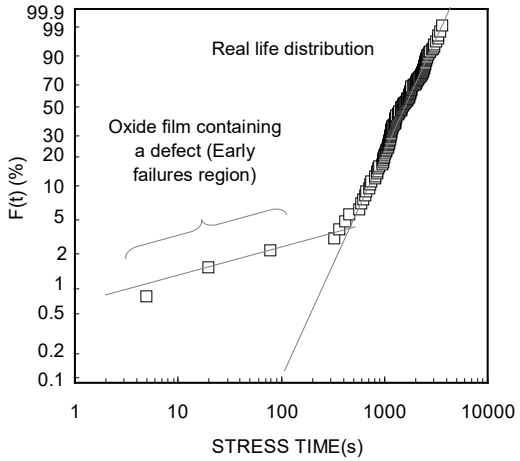

Figure 4-11 TDDB data distribution (Weibull)

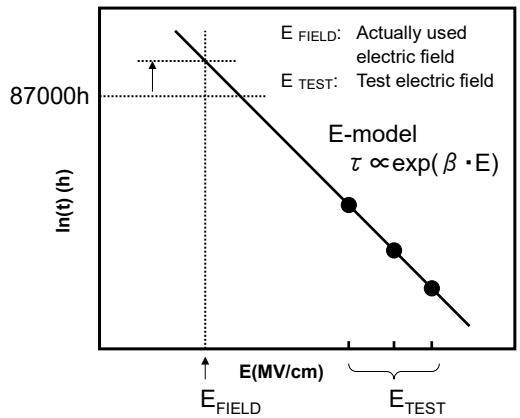

Figure 4-12 Electric field acceleration model and life prediction

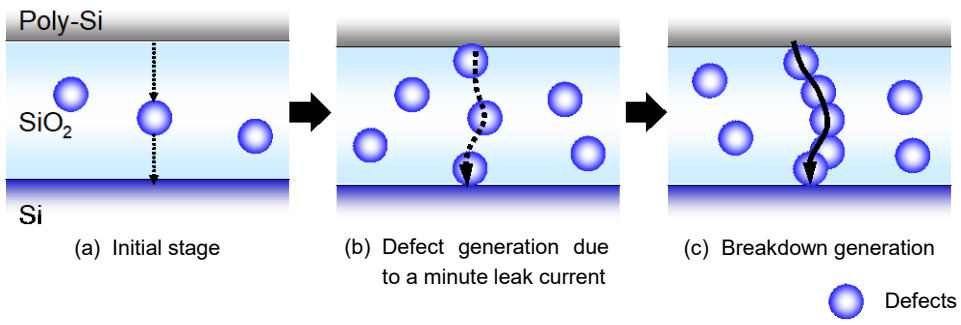

Figure 4-13 Gate insulation film failure model (percolation model)

4.2.2.2 Hot Carrier (HCI)

Hot carrier is a failure mechanism: electric charges (carriers) that have attained high energy accelerated by an electric field mainly inside the MOS FET are trapped in the gate insulation film, and this causes the transistor characteristics to fluctuate to cause a circuit operation error. In a general operating environment, the greatest transistor deterioration is caused by Drain Avalanche Hot Carrier (DAHC) injection, which occurs when electrons flowing through an NMOS FET channel are accelerated by the high electric field near a drain. On the other hand, the hot carrier mechanism that injects electric charges to insulation film is also used to write or erase data in non-volatile memory.

(1) Drain Avalanche Hot Carrier (DAHC) injection

Electrons flowing through an NMOS FET channel are accelerated by the high electric field near a drain and performs ionization (ionization collision) to generate electron-positive hole pairs. Characteristics fluctuation of transistors (such as threshold value fluctuation and decrease in drain current) caused by injection and trapping of carries having high energy among these pairs into gate insulation film is referred to as Drain Avalanche Hot Carrier (DHAC) injection. (See Figure 4-14.)

As for DAHC injection, electrons are mainly injected into gate insulation film of an NMOS FET, and the maximum deterioration occurs under the condition where the gate voltage is approximately $1/2 \cdot V_{DS}$. Therefore, in a CMOS circuit, hot electron injection occurs when the signal is inverted (H→L/L→H), so that deterioration progresses as the circuit is operated.

This problem can be avoided by selecting operating conditions (voltage, duty) under which hot carriers are not easily generated in the circuit design stage, and reliability can also be improved by providing circuits with the required operating margin. As a countermeasure on the side of a device, for example, a device structure (LDD structure) that suppresses hot carrier generation by relaxing the electric field around drains is used.

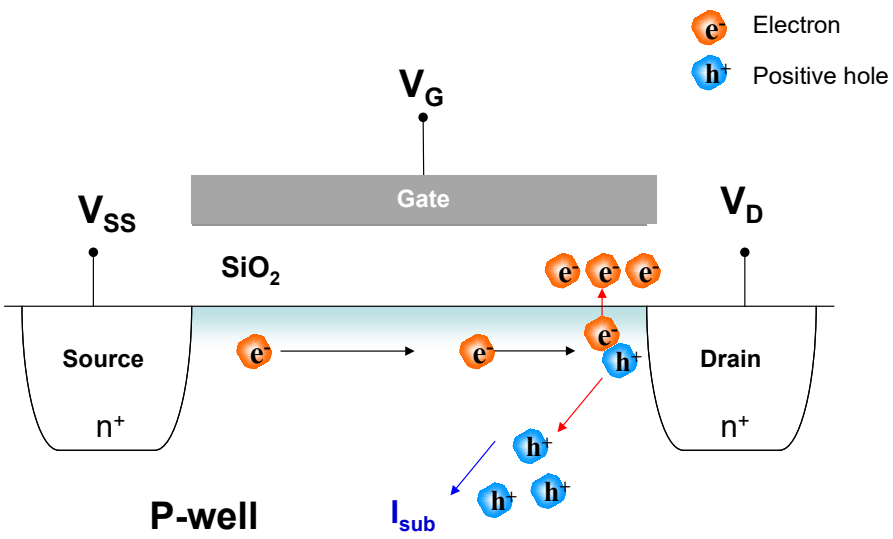

Figure 4-14 DAHC mechanism

4.2.2.3 Negative Bias Temperature Instability (NBTI)

Negative bias temperature instability (NBTI) of a PMOS FET is the following phenomenon: transistor characteristics fluctuate when a negative gate bias is applied to a PMOS FET. This is one of the transistor deterioration mechanisms known as a "slow trap." Since surface channel type transistors are used in a PMOS FET that uses the latest MOS processes, deterioration is increased, and this is a transistor reliability problem as well as hot carriers.

(1) NBTI deterioration mechanisms

When a negative bias is applied to a PMOS FET, positive holes on the Si surface are trapped by the Si-H bond of the Si-SiO_2 interface, and hydrogen (H) disassociates from the Si-H bond and an interface state is generated. The hydrogen disassociated from the Si bond diffuses into the gate insulation film and is trapped within it, and then generates a positive fixed electric charge. In this way, deterioration of the transistor characteristics progresses.

$$\mathrm{Si \equiv Si\text{-}\ H + hole \Leftrightarrow Si \equiv Si\text{-}\ \cdot^{+} + H}$$

$$\mathrm{H + H \Leftrightarrow H_2}$$

The interface state generated on the interface between the Si and the gate insulation film traps the positive electric charges when the PMOS FET operates, and it is electrified with the positive charge. This causes the transistor threshold voltage (Vth) to fluctuate and lowers the drain current together with positive fixed electric charges generated in the insulation film.

As one characteristic of NBTI, when a negative bias is applied to a gate, deterioration occurs regardless of transistor operation, so deterioration proceeds even in circuits that are not operating. On the other hand, the following phenomenon also occurs:

fluctuated characteristics recover rapidly when negative bias stress is not applied to the gate, and it is already found that the amount of fluctuation in the operating state is hardly dependent on the operating frequency. As the process conditions, the amount of NBTI deterioration is closely related to the concentrations and profile of impurities (such as N, H and B) contained in the gate insulation film, and especially gate insulation films (SiON, SiN) containing a large amount of nitrogen (N) deteriorate greatly.

As the methods for avoiding this problem, the following measures can be taken in the design: the circuit operation is designed to have sufficient margin by taking into consideration transistor deterioration, and the electric fields applied to gate insulation film is designed to be lowered. Countermeasures in devices are also taken such as forming of the gate insulation film that cannot generate interface states or fixed electric charges easily.

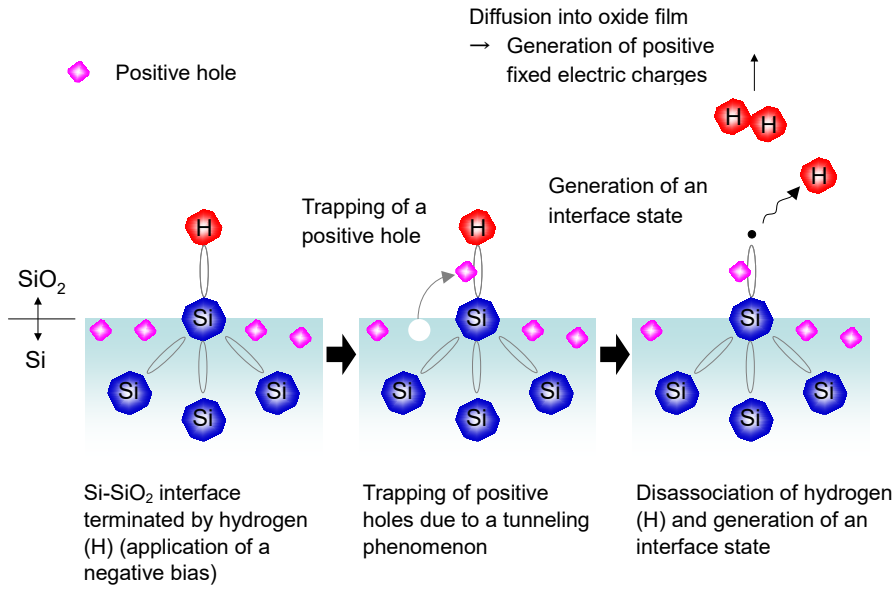

Figure 4-15 NBTI failure mechanism

4.2.2.4 Soft Error

When α rays, high-energy neutron rays generated due to cosmic rays and so on enter semiconductor devices such as a memory element, large amount of electron-positive hole pairs are generated in the silicon crystals. These electric charges invert the memory nodes, and this causes memory data errors known as a soft error phenomenon. The soft error is the following phenomenon: memory data and/or logic circuit data are (is) temporarily inverted. This error can be recovered by rewriting the data. Although this phenomenon previously occurred in DRAM, it is currently also considered as a problem of the SRAM reliability.

(1) Principle of generation of a soft error by α rays

Quartz materials used in resin-sealed packages of semiconductors contain a trace amount of radioactive elements (uranium: ^{238}U, thorium: ^{232}Th). In addition, some lead bumps used in flip chips contain polonium (^{210}Po). When the high-energy α rays emitted from these radioactive elements enter the silicon substrate, electron (e-) and hole (e+)

pairs are generated along the α ray path inside the silicon. The electric field causes electrons generated inside a depletion layer to move to the n diffusion region and then collect them, and this lowers the electrical potential of the storage node capacitance. (See Figure 4-16.)

Figure 4-17 shows the soft error mechanisms of an SRAM memory cell. When the potential of the memory node on the High side is lowered below the threshold value of the driver transistor, both of two inverters forming a Flip-Flop are set to OFF at the same time, and this makes the Flip-Flop unstable and causes it to malfunction. Generally, when the word line is selected, the memory node potential (Vh) on the High side is lowered to Vcc - Vth (word transistor threshold value). When the word line is not selected, the memory node on the High side is charged through the load of the memory cell and the potential returns to Vcc. The shorter this recovery time from Vcc - Vth to Vcc is, that is, the larger the current supply capacity of the load of the memory cell is, the more the soft error resistance is improved.

As a countermeasure against soft errors caused by α rays, α ray emission level is reduced, for example, by forming of a protective film on the chip surface to absorb α ray or by using highly pure package materials containing less radioactive elements.

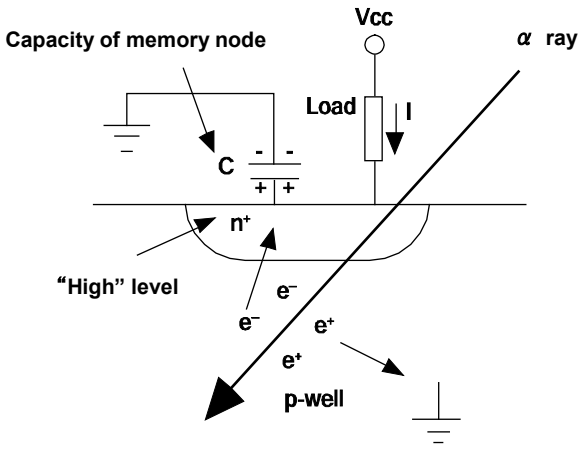

Figure 4-16 Generation of electron – positive hole pairs due to α rays

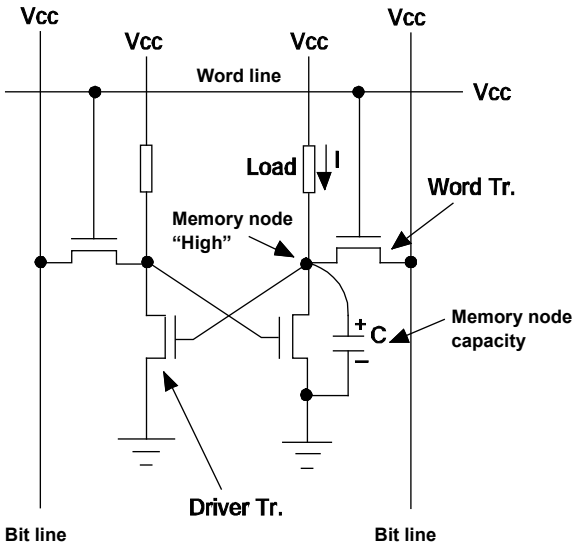

Figure 4-17 Soft error of an SRAM cell

(2) Soft errors due to cosmic rays

In the atmosphere, high-energy cosmic rays collide with atoms that comprise the atmosphere to generate high-energy protons and neutrons. When these high-energy neutrons pass through silicon, electron-positive hole pairs are generated along the path of these neutrons or these neutrons collide with silicon atoms to generate secondary ions by spallation reaction, and these actions cause soft errors. Since the arriving amount of high-energy neutrons generated by cosmic rays varies depending on the geographical conditions and increases in a region of a high altitude whose covering effect with the atmosphere is low, it is noted that the soft error occurrence rate increases in such a region. This may cause serious reliability problems in applications such as aircrafts and satellites.

Since it is difficult to suppress factors causing soft errors caused by cosmic rays, these soft errors are known as failure mode that occurs at the fixed probability. As the countermeasure method for this problem, an error correcting code (ECC) is added to an SRAM so that data where a soft error has occurred can be corrected. In addition, device structures such as SOI structures that are resistant to the effects of soft errors are also used in some cases.

4.2.2.5 Electromigration

Electromigration is a failure mechanism: electrons flowing through metal (Al, Cu) wiring physically collide with the metal atoms, and this causes the metal atoms to migrate (move) and form voids in the wiring, then leads to increase in the wiring resistance and/or disconnection of the wiring. Electromigration is a key failure mechanism that determines the long-term reliability of wiring.

(1) Electromigration in aluminum wiring

When thin film used in aluminum (Al) wiring is formed by spattering, aluminum atoms are integrated in a polycrystalline (grain) structure. (See Figure 4-18.) When a prescribed current or more flows through this wiring, an electromigration phenomenon occurs where metal atoms physically move as a result of stress generated with collisions between the electrons and the metal atoms. The metal atoms around the grain boundary move easily because their binding energy is small. If the wiring contains ununiform sizes of grains, electromigration occurring at the grain boundary causes voids to grow along the grain boundary, and this leads to disconnection of the wiring. (See Figures 4-19 and 4-20.)

As a countermeasure against this problem, a trace of copper is added to aluminum wiring in the process to delay movement of aluminum atoms and then suppress it or the top and bottom of wiring are covered with metal alloy (barrier metal) such as Ti and W to suppress aluminum atom movement. The current density that flows in the wiring is restricted to a certain value or less as a countermeasure in the circuit design stage.

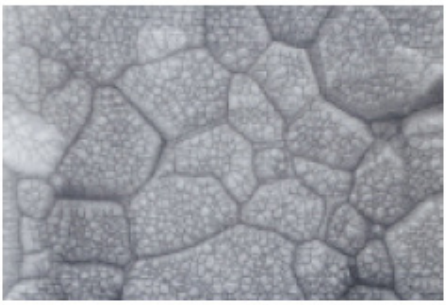

Figure 4-18 Grain structure of the aluminum wiring

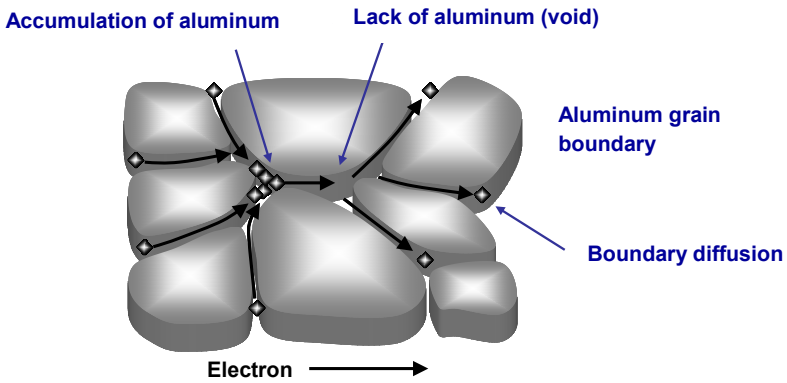

Figure 4-19 Electromigration mechanism

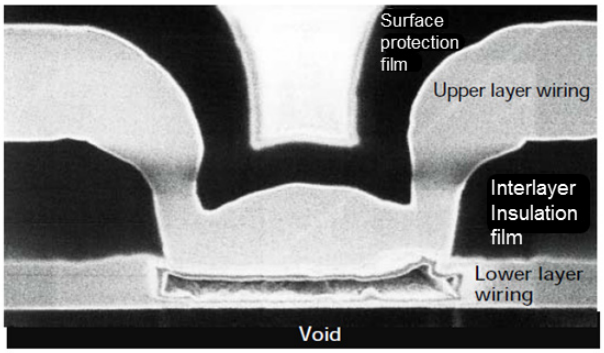

Figure 4-20 Photograph of electromigration

(2) Electromigration in the copper wiring

Copper wiring is formed in an embedded wiring (damascene) process that uses electrolytic plating. The melting point and activation energy of the copper wiring are higher than those of the aluminum wiring, and the copper wiring shows the reliability with respect to electromigration that is several ten to several hundred times higher than that of the aluminum wiring. However, miniaturization of wiring in the up-to-date processes causes the current density to increase, so electromigration durability is becoming an important challenge related to the reliability.

The electromigration resistance of copper wiring is known to be greatly affected by the crystal grain size and orientation and the interface adhesion between the copper and the barrier metal. Especially, in case of the copper wiring that has a structure surrounded by barrier metal, when the level of adhesion between the copper on the top surface to be flattened and the cap layer is lowered, the copper at the interface moves easily, and then this leads to migration. Therefore, it is important to take the measures for improving the adhesion level of the interface between the copper and the cap layer in the process. As for circuit design, measures for this problem is also taken such as decreasing of the current density flowing to the wiring to a certain value or less.

4.2.2.6 Stress Migration

Stress migration is a failure mechanism: stress applied to metal wiring causes metal atoms to creep, and then voids to occur in the wiring to lead to increase in the resistance or disconnection of the wiring. Stress is generated in the metal wiring (Al, Cu) used in LSI due to temperature differences between the heating process of the manufacturing process and the usage environmental temperature. Due to this stress, vacancies in the metal wiring cause a creep phenomenon and converge in a single location to form a void.

Stress migration occurs because of the interaction between the wiring stress and the metal atom creep phenomenon. The higher the temperature becomes, the faster metal atoms creeps. On the other hand, the higher the temperature becomes, the less stress applied to the metal wiring becomes. It is, therefore, known that there is a peak to the temperatures at which stress migration occurs.

(1) Aluminum stress migration

Since many aluminum atoms that have defects or whose bonding force is weak exist at the grain boundary of the polycrystalline structure in the aluminum wiring, when tensile stress is applied to the wiring, these aluminum atoms or defects at the grain boundary causes a creep phenomenon, then forms voids. Voids generated in the aluminum wiring by the tensile stress grow mainly along the crystal grain boundary, and may lead to increase in the resistance or disconnection of the wiring. (See Figure 4-21.)

Generally, the occurrence rate of aluminum stress migration is said to have a peak around 150 to 200°C, and this may become a problem for long-term reliability of devices that are supposed to be used for a long time under a high temperature environment.

As a countermeasure against this problem, a pattern design is made so that any excessive stress cannot be applied to the wiring. Stress migration can be prevented when the aluminum wiring structure whose top and bottom are laminated with the barrier metal (such as Ti and W) is used. In addition, countermeasures such as use of an interlayer film structure that relaxes stress and optimization of the heating process are also taken to reduce the residual stress of the wiring.

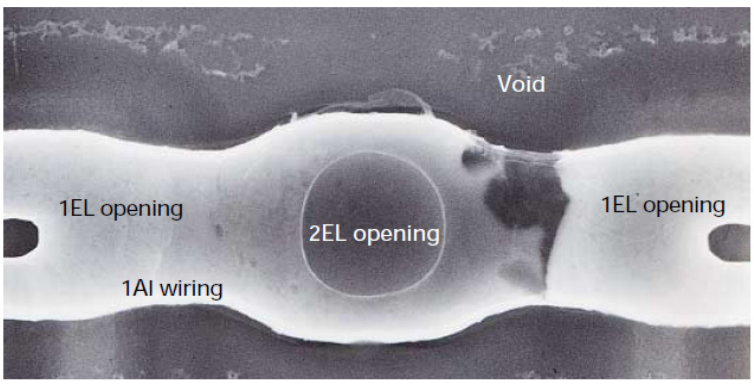

Figure 4-21 Disconnection failure caused by stress migration of aluminum wiring

(2) Stress migration of copper wiring

In case of copper wiring stress migration, Stress Induced Voiding (SIV) mode in which voids occur at the via portion that connects the upper wiring and the lower wiring is a problem for reliability. When wide wiring and narrow wiring are connected by a single via hole, tensile stress on the wide wiring side is concentrated on the via hole, and this causes a defect in the copper wiring to move to the via portion due to a creep phenomenon, and then generates a void. (See Figure 4-22.) Occurrence of stress migration at a copper via hole is known to have a temperature peak around 200 °C. However, since this failure is greatly dependent on stress generated in the high-temperature annealing process after formation of the copper wiring and it occurs in a short time, it causes an early failure.

As a countermeasure against this problem, the wide wiring and the narrow wiring are connected by two or more via holes in the design stage. When the wirings are connected by two or more via holes, stress applied to one via hole is relaxed and any void does not occur even though stress is applied to the other via hole intensively to cause a void to occur. This can, therefore, prevent open defects between wirings. As a countermeasure against this problem in processes, measures such as those for relaxing the stress of the copper wiring and for selecting the process conditions that reduce defects of the copper wiring are taken.

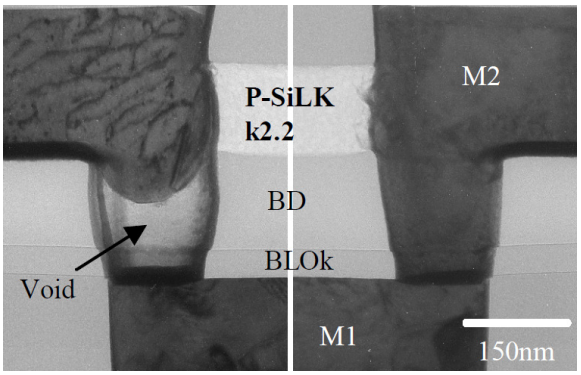

Figure 4-22 Void occurring due to stress migration in a via hole of the copper wiring

<Reference material>

1) R. Kanamura et al.: Symp. on VLSI Tech., p. 107, 2003

4.3 Reliability Test

In this chapter, we will explain environmental and endurance tests.

Mainly, we will describe basic life tests and those test methods which have recently been watched with interest.

4.3.1 High Temperature Operating Life

High temperature operation test simulates an operating life of a semiconductor device under acceleration condition under high temperature bias condition. Although the test conditions may vary depending on the assumed market environment, temperatures of 125 °C and 150 °C are often used (it is important to select the test temperatures within the range where Tj does not exceed the limit value). This test is mainly aimed at verifying the service life against the failure mechanism accelerated by electric field, current, and temperature (TDDB, EM, NBTI and the like).

The test is effective for grasping the majority of faults except for faults related to mechanical strength, humidity susceptibility, and ESD tolerance.

Conventionally, since HCI (hot carrier injection) deterioration has a negative activation energy, low temperature operation test was considered effective. However, in the latest devices, HCI deterioration often has positive activation energy and therefore, high temperature operation test may be effective for HCI depending on the process.

Acceleration with respect to temperature is described in the HAST section. Generally speaking, in accordance with Arrhenius theorem (see 4.4.1 Acceleration model under environmental stress for details), it may be better to consider that the acceleration with respect to voltage depends not only on the voltage but also on the electric field for some device subject to deterioration.

4.3.2 Temperature Humidity Bias

This test is aimed at grasping the lifetime of a semiconductor device in a high humidity environment and it is performed under the conditions where the deterioration reaction of moisture propagating to a semiconductor chip mainly using a moisture permeable sealing material and a glass sealing material as a route and a semiconductor is accelerated. In general, 85°C85%RH are often selected as the test condition. However, depending on the constituent materials of the device, other conditions such as lower temperature may need to be taken into consideration. Unlike a simple humidity test, this test is performed in a state where power supply is active, and therefore, it is also possible to check the fault tolerance caused by electrochemical reaction caused by impurities being ionized by water and electric field (galvanic corrosion, ion migration and the like).

Acceleration of humidity is derived by relative humidity model and absolute water vapor pressure model.

Prior to the test, it is necessary to decide the continuous and intermittent supply of the power while taking into consideration the self heating of the device. Further, during the test, careful attention must be paid to dew condensation produced on the seal glass due to sudden temperature drops upon taking out the test sample from the test tank. In order to avoid such undesirable situation, measures should be taken including removing unnecessary moisture in the high humidity air circulation passage of the test tank and taking out the test sample after the temperature and humidity drop sufficiently.

4.3.3 Temperature Cycling

Semiconductor devices are made up of multiple materials. Especially their packages realize a complicated structure with multiple materials. Each of these constituent materials has an inherent thermal expansion coefficient, and mechanical stress is caused by temperature changes. When exposed repeatedly to high temperature and low temperature, the semiconductor devices will repeat expansion and contraction and mechanical stress will be repeated at the same time.

These tests are conducted for the purpose of checking the resistance of devices to these stresses as well as the lifetime of devices.

This test enables detection of faults such as peeling of bond part of two different materials with large difference in thermal expansion coefficient (seal glass, etc.).

Regarding the acceleration, "the power law" is generally used with a temperature difference as one factor. However, in some cases including the case of low cycle thermal fatigue of a material, the strain amplitude due to temperature difference may be used as a factor (see 4.4.1 Acceleration model in environmental stress).

In addition, minor rules should also be taken into consideration upon calculation of market life. In the S-N diagram used in the minor rule, fatigue failure does not depend on the number of stress in the case of stress below the fatigue limit.

In other words, when the stress in the market (temperature difference) is small, it means that the stress given by the temperature cycle test may cause failure, but the device may not fail in the actual market environment.

4.3.4 PTC

PTC is an abbreviation for Power and Temperature Cycling, and it is the test method for checking the worst temperature environmental tolerance of a semiconductor device by changing its operation and the temperature-environment periodically.

This is an evaluation method classified as a composite test, which has gained considerable attention recently, and it consists of a power cycle test that has been used for a power device and a temperature cycling test that has been used for general semiconductor devices. It is a test method for evaluating the reliability of connection. When operation of the device is monitored during this test as well as the reliability of connection, the operation test can be conducted in the entire temperature range from a low temperature to a high temperature.

Products for which this test is conducted are semiconductor devices whose power has to be turned on or off in the entire temperature range within an operation guarantee range. In particular, products that are supposed to be used under the environment whose temperature varies drastically such as outdoor environment are tested. For example, semiconductor devices for vehicle that meet the AEC-Q100 requirements have to be tested. According to the AEC-Q100 requirements, products whose power is 1 W or more or satisfies the expression $\Delta Tj \geqq 40°C$ has to be tested.

JEDEC JESD22-A105 is used as the test standard, and the JEDEC standard is used as the reference standard of the AEC-Q100 requirements also.

- JEDEC standard test conditions

Table 4-3 Standard test conditions *1

Test Condition	Temperature Extremes Degrees C.	Transition Time Between Temp Extreme, Max.	Dwell Time at Each Temp Extreme, Min.
A	-40 (+0, -10) to +85 (+10, -0)	20 minutes	10 minutes
B	-40 (+0, -10) to +125 (+10, -0)	30 minutes	10 minutes

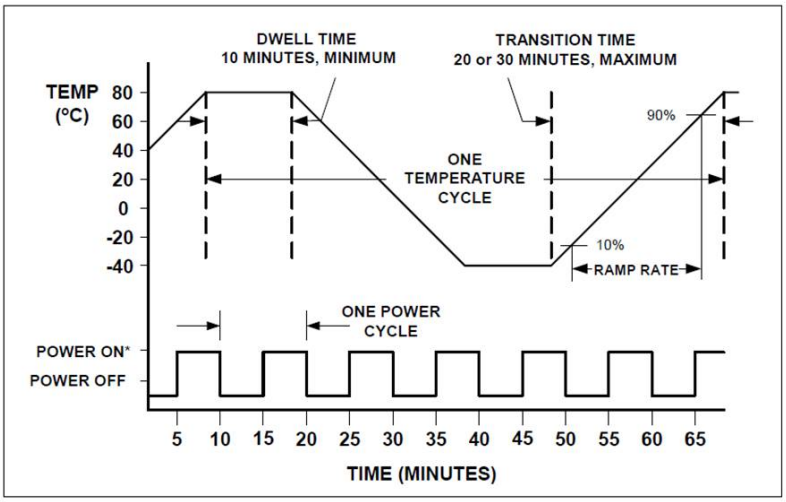

Figure 4-23 Power temperature cycling standard test conditions [*1]

*1: From JESD22-A105C, ©Copyright JEDEC. Reproduced with permission by JEDEC.

- AEC-Q100 Standard test conditions [*2]

  Grade 0: Ta of -40 °C to +150 °C for 1000 cycles.

  Grade 1: Ta of -40 °C to +125 °C for 1000 cycles.

  Grades 2 and 3: Ta -40 °C to +105 °C for 1000 cycles.

  * 2: AEC-Q100-Rev-H Page 11

  The following failure modes and reliability problems are assumed to occur.

  - Fracture or breakage caused because the coefficient of thermal expansion (CTE) varies depending on the constituent materials
  - Connection reliability
  - Abrupt local heating caused due to power-on/power-off under the ambient temperature environment
  - Failure caused by cold starting

4.3.4.1 Notes on Testing

- Precondition (PC)

  The following necessary preprocesses have to be executed before testing a device.

- Temperature rise rate/drop rate of the temperature cycle (referred to as “ramp rate” hereinafter)

  The ramp rate 15°C/minute or less has to be applied to a semiconductor device connected with solder or a package whose heat capacity is large and whose thermal conductivity is low.

- Package temperature and junction temperature

  Since high-power and high-heat-generating semiconductor devices are to be tested, the package temperature and/or junction temperature may become drastically higher than the ambient temperature when the devices are tuned on. The test has to be conducted so that the package temperature and the junction temperature cannot exceed their respective maximum ratings.

- Check of the device operation when the test is conducted

  The system for always monitoring the operation condition of semiconductor devices to detect a malfunction/failure of the devices is required.

4.3.5 Highly Accelerated Temperature and Humidity Stress Test (HAST)

HAST is conducted as an acceleration test for evaluating the humidity resistance to know the life of a device under the high temperature and high humidity conditions.

Since power is supplied to semiconductor devices at high temperature and high humidity, malfunctioning such as corrosion and ion migration of metal wiring can be detected in the early stage.

For an acceleration model caused by the temperature, the absolute water vapor pressure or the relative humidity is used as an acceleration factor.

The accelerating factors for confirming moisture resistance is rarely applied only with humidity, and it is evaluated using both temperature and humidity.

This operation has to be performed to promote reaction related to the humidity, and it leads to acceleration of the humidity stress as a result.

As for the acceleration model in relation to humidity, the absolute water vapor model as well as the relative humidity model that can be expressed as a product of the power law and the Arrhenius law of relative humidity are often used. Details are explained in 4.4.1 Acceleration model in environmental stress.

4.3.5.1 Differences from the Temperature/Humidity Bias (THB) Test

During the HAST, the temperatures that are used exceed the boiling point of water and in the HAST, the temperatures are more highly accelerated than in the THB test where the boiling point of water is raised by higher pressure inside the test tank to realize high temperature and high humidity environment.

In high acceleration HAST, consideration must be given to the test temperature, the resistivity of pure water used for the test, the glass transition temperature of the constituent materials, etc. so as not to cause failure outside the purpose of the test.

4.3.5.2 Recent Trend of This Test

As an acceleration test of humidity resistance, HAST as well as a THB test has been accepted gradually. However, since conventional HAST equipment exhausts air from its test tank, the environment inside the tank is different from that of the THB test equipment, and HAST has not been best suited for evaluation of metal oxidization.

Recently, HAST test equipment has been developed with considering influence of oxygen without exhausting any air from its test tank.

4.3.5.3 Consideration to the Test

Since HAST shall be conducted in the high temperature and high humidity environment, it may cause a semiconductor device to generate dew condensation, so we have to prevent dew condensation from being generated inside the test tank. In addition, when a semiconductor device is taken from the test tank, abrupt temperature change may generate dew condensation. Therefore, the measures for preventing dew condensation have to be taken such as control of the temperature inside the test tank so that the temperature can be equal to or lower than the room temperature.

Examples of a failure caused by dew condensation are as follows: oxidation of a terminal of a semiconductor device and degradation of the optical characteristics caused by dew condensation on the optical path of a hollow package.

Note that in case of a hollow package, when a semiconductor device is taken out without lowering the water vapor pressure or temperature/humidity gradually, decompression inside a hollow may cause the package to be deformed.

4.3.6 Tumble Test

A tumble test is one of drop test methods, and it repeatedly rotates and drops a sample set inside the regulated tumbling barrel to reproduce the effect of drop impact on a product being used and evaluate it. This test is standardized by the standards such as IEC 60068-2-31 (2008) and JIS C60068-2-31 (2013), and is applied to small and lightweight cellular devices such as a smartphone, handy terminals, displays and module products into which these devices are incorporated. Mainly customers in Europe request this test to be conducted strongly. Normal natural drop test drops a sample with superior repeatability while controlling the posture of each plane, corner and edge of the sample. In the other hand, the behavior of a sample located in the tumble barrel is not always uniform in case of the tumble test, so that this test is referred to as random drop test also. It is, therefore, supposed to be useful to detect an unexpected failure or reproduce a failure occurred in the market. Although the test requirements and severity applied to this test seem oppressive, this test has become established as a test method for classifying the durability and robustness of products.

The specifications of test equipment are regulated according to the International Standards described above, and one example of equipment is shown in Figure 4-24 below (drop height: 1 m). Note that since the specifications of the example may not be applied to your equipment as they are depending on the shape and/or weight of the actual sample.

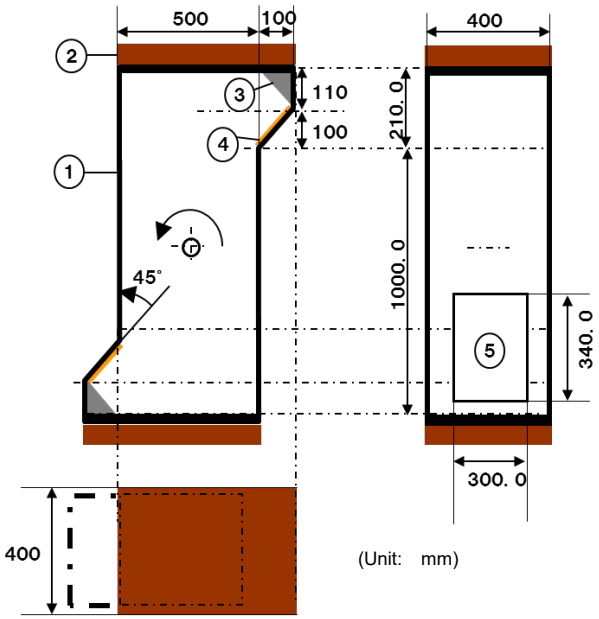

Figure 4-24 Tumble tester (example)

(Supplementary information for Figure 4-24)

① The body of a rotor is made of steel sheet (which is stainless steel, and referred to as “steel sheet” hereinafter)1.5-mm in thickness.

② The floor on which a sample drops shall be 3 mm in thickness and a flat and fixed steel sheet, and be backed with a wood plate 10 to 19 mm in thickness.

③ To stop a sample between two consecutive drops, wedge-shaped rubber whose hardness is regulated is attached.
80 ± 20 IRHD hardness (JIS K 6253-1993; Vulcanized rubber hardness test method)

④ The sliding surface inside the tumbling barrel shall be made of a smooth and hard plastic plate such as an acrylic plate, and its inclination angle shall be 45 degrees.

⑤ A door made of a transparent acrylic resin plate shall be provided at the opening of the tumbling barrel.
The typical test conditions and severity are described in Table 4-4. The rotation speed is approximately 5 to 6 rpm, and it is desired that the speed shall be decided after observing the behavior of a sample inside the tumbling barrel with a device such as a small camera so that the sample cannot collide against the side of the inside of the tumbling barrel (for securing 1.0-m drop distance) (see Figure 4-25).

Table 4-4 Typical tumble test conditions and severity

Drop height	1.0 m
Rotational speed	Approximately 5 rpm *
Severity	100 drops (50 rotations)

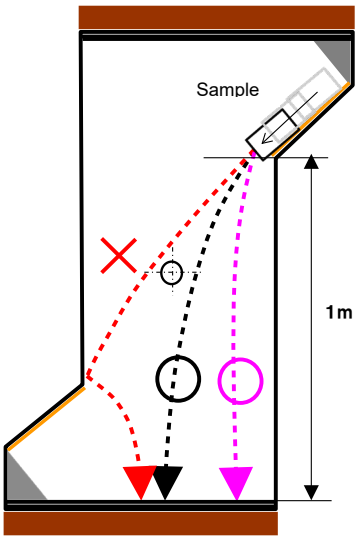

Figure 4-25 Drop behavior of a sample

(Supplementary information for Figure 4-25)

The rotational speed of the tumbling barrel has to be selected so that any sample cannot collide with the internal surface of the tumbling barrel.

The lighter a sample is or the higher the rotational speed is, the more likely the sample collides with the side of the tumbling barrel. Note that rebounding or any other reaction of a sample after it drops is not regulated, and its control is supposed to be difficult.

4.4 Acceleration Models

Generally, failures of parts including semiconductor devices are generated by response of an atom or something of a molecular level, and they can be described according to Eyring's absolute reaction kinetics (referred to as "Eyring model" hereinafter).

In the temperature range where the absolute temperature T should be noticed regarding the reliability, the life time L of this Eyring model is represented by the following separable differential equation, where the activation energy shown in Figure 4-26 is Ea, stress causing a malfunction other than the temperature is S, and a Boltzmann constant is k (8.617×10E – 5 [eV/K]).

$$L = A \cdot S^{-n} \cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.1}$$

"A" and "n" are constants in the expression above.

The overview of the acceleration models regarding environmental stress and operational stress that are used in semiconductor devices is described below.

4.4.1 Acceleration Model Regarding Environmental Stress

(1) Temperature acceleration model

Since a part "exp(Ea/kT)" on the right side of the expression 4.4.1 above is the same as the expression empirically derived by Arrhenius in the 19th century, this model is referred to as an Arrhenius model too.

Ea indicates activation energy, and eV is used as a unit. Activation energy is required to make a chemical or physical reaction progress, and [ev] is generally used as a unit in case of semiconductors. When the chemical and physical reactions of the failure mechanisms are the same as each other, the activation energies are inevitably the same as each other.

$$L = A \cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.2}$$

(2) Humidity acceleration model

In case of an acceleration model derived from the humidity, the absolute water vapor pressure V_p or the relative humidity RH is indicated as humidity stress.

The typical models are shown below.

① Absolute water vapor pressure model

This a model where temperature stress and humidity stress are indicated with the absolute water vapor pressure V_p, and it is known to adapted empirically. Since V_p is subject to the temperature, it cannot be described in an Eyring model.

$$L = V_P^{-n} \quad \cdots \text{ Expression 4.4.3}$$

② Relative humidity model

Since V_p is subject to the temperature, this is represented so that it can conform to an Eyring model by separating variables, the absolute temperature T and the relative humidity RH, and this is equivalent with the expression 4.4.1, where S = RH.

$$L=A\cdot (RH)^{-n}\cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.4}$$

③ Lycoudes model

There are models where a temperature function, a relative humidity function and a voltage function are multiplied. A model reported by N. Lycoudes and referred to as a Lycoudes model is described below as a typical model.

$$MTTF=A\cdot \exp(Ea/kT)\cdot \exp(B/RH)\cdot V^{-1} \quad \cdots \text{ Expression 4.4.5}$$

In the expression above, V indicates voltage, and B indicates a constant.

(3) Temperature difference acceleration model

This model is applied to a failure caused by repetitive application of stress generated due to temperature difference (thermal stress), and the corresponding number of cycles N is represented by the following expression when the temperature difference is ΔT and S = ΔT is described in the expression 4.4.1.

$$N=A\cdot \Delta T^{-\alpha} \quad \cdots \text{ Expression 4.4.6}$$

[Supplementary information]

When an inelastic distortion amplitude is Δεin low cycle fatigue, a failure Nf (cycle life) caused by thermal fatigue of material conforms to the Coffin-Manson model of the following expression.

$$\Delta\varepsilon\cdot Nf^{\alpha}=C \quad \cdots \text{ Expression 4.4.7}$$

In the expression above, αand C are constants of the material.

In low cycle fatigue, failures caused by repeated thermal stress conform to a Coffin-Manson model, and a temperature difference acceleration model is one of the Coffin-Manson models. When a semiconductor chip malfunctions, it can be described with a temperature difference acceleration model in many cases. However, when a mounting failure including a package occurs, a Coffin-Manson model has to be considered like in the case of the thermal fatigue life of a solder bump joint. A deformed expression of a Coffin-Manson model revised due to the effect of the temperature cycle frequency and the maximum temperature that were pointed out by Norris or other people is shown below.

$$Nf=C\cdot f^{m}\cdot \Delta\varepsilon^{-n}\cdot \exp(Q/kT_{MAX}) \quad \cdots \text{ Expression 4.4.8}$$

In the expression above, Nf indicates a fatigue life, C indicates a material constant, m and n indicate indexes, f indicates a repetition frequency, Δε indicates an inelastic distortion amplitude, Q indicates activation energy, k indicates a Boltzmann constant, and TMAX indicates the maximum operating temperature.

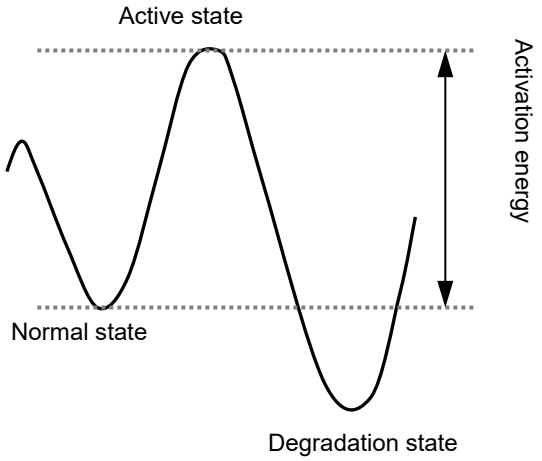

Figure 4-26 Activation energy

4.4.2 Acceleration Model Regarding an Operational Stress

Voltage, current, electric field strength and current density are examples of the operational stresses deciding the life of semiconductor devices. As described in Section 4.2.2, the operational stress varies depending on the failure mechanism. Acceleration models regarding the main failure mechanisms are described below.

Note that the lives of semiconductor devices for the failures described below (1) to (4) are described by Eyring models of operational stress and temperature stress since these lives vary depending on the temperature.

(1) Acceleration model of gate oxide film time-dependent dielectric breakdown (TDDB)

The life of a device (TTF: time to failure) caused by TDDB varies depending on the thickness of a gate oxide film. The following combinations shall be appropriate: Eox model for the thickness 5 nm or more, Vg model for the thickness from 2 nm to 5 nm, and Power-law model for the thickness less than 2 nm.

① Eox model

$$TTF = A \cdot \exp(-\gamma_{EOX} \cdot Eox)\ \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.9}$$

② Vg model

$$TTF = A \cdot \exp(-\gamma_{Vg} \cdot Vg)\ \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.10}$$

③ Power-law model

$$TTF = A \cdot Vg^{n} \cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.11}$$

In the expressions above, γ_{EOX} indicates an electric field strength acceleration coefficient, γ_{Vg} and n indicate voltage acceleration coefficients, Eox indicates a stress electric field applied to a gate, and Vg indicates the stress voltage applied to a gate.

(2) Hot Carrier (HC) acceleration model

The life of a device affected with the hot carrier is classified into a board current model described with board current and a 1/ Vds model described with drain voltage. A process node after a 0.25 um and 0.15 um generations is greatly affected with elements other than board current, and a 1/ Vds model tends to be applied to a device.

① Board current model

$$TTF = A \cdot Isub^{-m} \cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.12}$$

② 1/Vds model

$$TTF = A \cdot \exp(B/Vds) \cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.13}$$

In the expression above, m indicates a board current dependency coefficient, B indicates a voltage dependency coefficient, Isub indicates the maximum board current when stress is applied to a device and Vds indicates the drain voltage when stress is applied to a device.

(3) Negative Bias Temperature Instability (NBTI) acceleration model

The life of a device regarding NBTI is frequently represented by an expression like those shown below.

$$TTF = A \cdot \exp(\gamma \cdot Eox)\ \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.14}$$

$$TTF = A \cdot Eox^{\gamma} \cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.15}$$

$$TTF = A \cdot Vg^{n} \cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.16}$$

In the expressions above, γ indicates an electric field acceleration coefficient, n indicates a voltage acceleration coefficient, Eox indicates the electric field strength applied to gate oxide film, and Vg indicates the voltage applied to gate oxide film.

(4) Electromigration (EM) acceleration model

As for theoretical treatment of the EM life, the Huntington expression is generally used.

$$\partial C/\partial t = D\nabla\{\nabla C - (eZ^*/kT)\ E \cdot C\} \quad \cdots \text{ Expression 4.4.17}$$

In the expression above, c indicates the atom concentration, D indicates a diffusion coefficient, Z* indicates the valid atomic value, E indicates an electric field, e indicates the charge of an electron, k indicates a Boltzmann coefficient, and T indicates the absolute temperature.

As for the actual EM life (TTF), the Black expression empirically found is used commonly. T indicates the absolute temperature, j indicates the current density, Ea indicates activation energy, A indicates a proportion coefficient, n indicates a current density function, and k indicates a Boltzmann constant.

$$TTF = A \cdot j^{-n} \cdot \exp(Ea/kT) \quad \cdots \text{ Expression 4.4.18}$$

<Reference materials>

1) JEITA EDR-4704A: Application guide of the accelerated life test for semiconductor devise
2) JEITA EDR-4707: Report on Failure Mechanism of LSI and reliability test method
3) JEITA ETR-7014: Research Report on Effects of Voids on Reliability of Lead-free Solder Joints and Standard of Evaluation Criteria
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7) T. Gasser: Hot Carrier Degradation in Semiconductor Device
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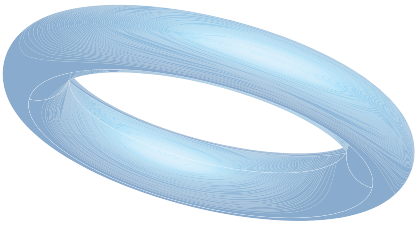
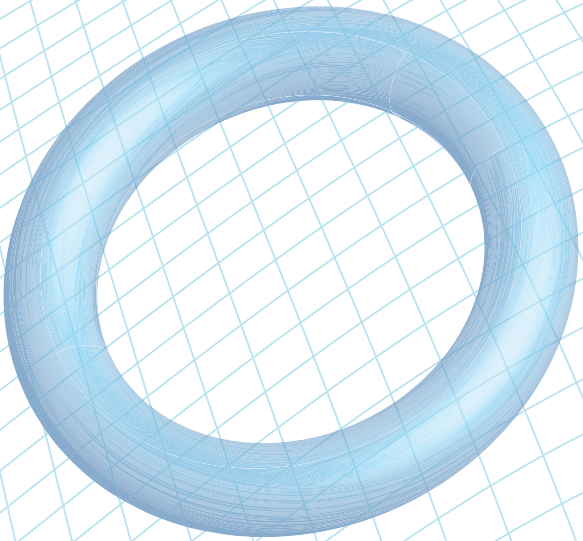
9) H. B. Huntington: Diffusion in Solids, Academic Press (1975)



Chapter 5 Failure Analysis Technologies



Chapter 5 Table of Contents

5.1 What is Failure Analysis?

Failure analysis consists of the following actions: checking the states of failures that occurred in the various manufacturing processes or the field, checking the product function and obtaining the electrical characteristics data with using semiconductor test equipment (such as a tester), and using the optimum physical and chemical methods and analysis equipment to identify the causes and mechanisms that led to the failures based on the check results and the obtained data.

5.2 Necessity of Failure Analysis Technology

We are at the leading edge of image sensors. Recently we have developed back side Illumination type CMOS image sensors and then stacked CMOS image sensors, and now manufacture stacked CMOS image sensors of a three-layer structure including even a DRAM in response to demands for large number pixel, highly sensitive and highly functional image sensors. As a result, manufacturing processes and product structures are becoming more complicated and diversified, and the corresponding failure causes and mechanisms are also diversified and becoming more complicated, which is unique to CMOS image sensors. Therefore, the higher-level analysis technology is required. On the other hand, extremely high level of quality and reliability are required for semiconductor devices. When manufacturing semiconductors, consistent quality and reliability must be built in them from the development stage to the manufacturing stage in order to prevent semiconductor devices from defect in the field or causing customers trouble.

It is, therefore, extremely important to swiftly analyze defect products detected in customers' processes or the field as well as those in each process such as development, manufacturing and reliability test processes, and provide feedback to the processes such as the manufacturing process and the design process through analysis of the cause and mechanism of malfunctioning to improve defect and product qualities. In this way, the failure analysis technology is essential for improvement of the quality and the product reliability and prevention of the same problem from occurring again through investigation of the cause and mechanism of various failures, and it contributes in unboundedly bringing the number of malfunctions close to zero in customers' sites and in the market.

5.3 Failure Analysis Technology

5.3.1 Role and Purpose of Failure Analysis

The rough flow of productization of semiconductor products is as follows: Development -> Prototyping -> Mass-production -> Shipment to the field. The roles and purposes of the failure analysis are: quickly and accurately identifying the cause of a failure occurring in each stage and feedback to each process to prevent the same failure from occurring again, and contribution in promoting a new process development, improving the yield, improving the reliability, improving the product quality and improving customers' satisfaction. (See Figure 5-1.)

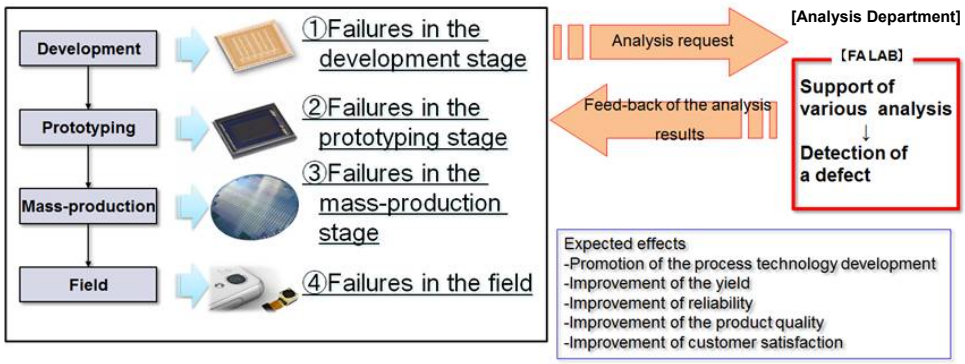


Figure 5-1 General productization flow and relevancy of analyses

5.3.2 General Failure Analysis Flow

The most important factor in failure analysis is how far the failure location can be narrowed down while still maintaining the failure symptoms. The failure cause identification rate varies widely depending on whether the failure location can be narrowed down only to the function block level having a certain degree of function or can be pinpointed (to the element level). Since the number of elements laminated to the block level has increased due to miniaturization of the semiconductor process recently, it is important to narrow down a failure location to the block level (circuit level) with non-destructive analysis securely, and then to the pinpointed level (element level) with destructive analysis. Finding a failure location with a radius of approximately several tens μm in the latest highly integrated semiconductor devices is comparable to searching for a coin dropped somewhere in a building with ten or more stories constructed in a site whose size is the same as that of a baseball stadium. In such a situation, it is impossible to find the location without any information simply by searching with only a vague notion of where to look. The possibility of finding the coin can be increased by following the procedure: carefully investigating the behavior and other details of the person who dropped the coin at first, narrowing the range of the location where the coin is thought to have been dropped as much as possible, identifying the location, and then searching the coin carefully. Narrowing down a malfunctioning point in a semiconductor device is similar with this searching procedure. It starts by using semiconductor test equipment (such as a tester) to execute a performance test or investigate the electrical characteristics to roughly narrow down the part of the device where the failure is likely to have occurred. (See Figure 5-2.)

[Phase 1] Reconfirmation of a failure mode

- Test technology

Use a test tool to confirm a failure symptom. Check the detailed electrical characteristics and plan the analytic approach.

[Phase 2] Fail Site Isolation

- Electrical analysis technology

Use the analysis technique appropriate for the electrical state to isolate a fail location such as a circuit node and an element.

[Phase 3] Identification of the cause of a failure

- Structure analysis technology

Identify a cause of failure by physically destroying a location where a failure is supposed to have occurred and observing it.

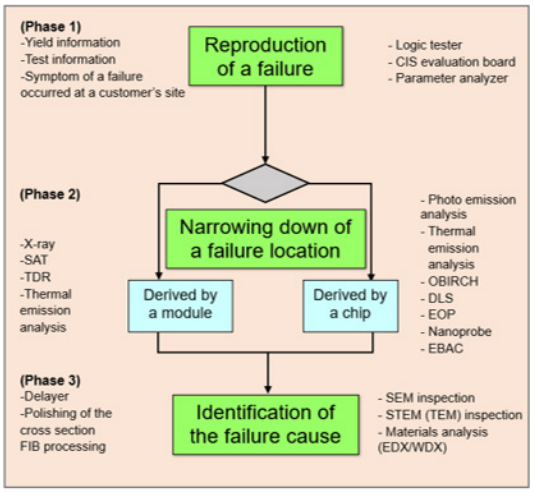


Figure 5-2 General failure analysis flow and equipment/analysis techniques mainly used

5.3.3 Investigation of failure occurrence states

When failures occur, under what circumstances a failure occurred is also extremely important information for estimating the failure cause and determining the failure analysis methods and procedures so that failure analysis can proceed smoothly. Therefore, when a failure sample is obtained, as much information as possible on that sample is gathered at the same time. Information on the environment in which the failure occurred (such as a place where the failure occurred, environmental conditions, circuits used, use conditions and mounting conditions.) is particularly helpful to estimate the failure mechanism and select analysis techniques and methods. In addition, such information is sometimes helpful to perform failure simulations and check reproducibility, and then to determine whether the failure occurred accidentally or due to a design problem.

5.3.4 Visual Inspection

To analyze a failure without disassembling the camera module on which a chip and a package or an image sensor are mounted, visual inspection is conducted to grasp the failure information. If the module has any characteristic abnormality, observing whether the light receiving element of especially the image sensor has any physical error with using an optical microscope or an electron microscope is useful to estimate where the failure occurred.

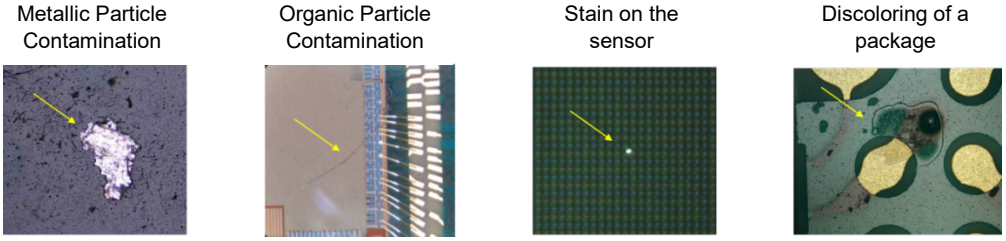


Figure 5-3 Typical failures

5.3.5 Evaluation of Electrical Characteristics

(1) Analysis by using a tester

If any failure whose cause can be estimated by the visual observation is not detected, electrical characteristics analysis is conducted to estimate where the failure occurred or its symptom. First, imaging characteristics of an image sensor is tested under the environment similar with that when the image sensor was shipped, and then the cause of the failure is estimated from the failure condition and characteristics.

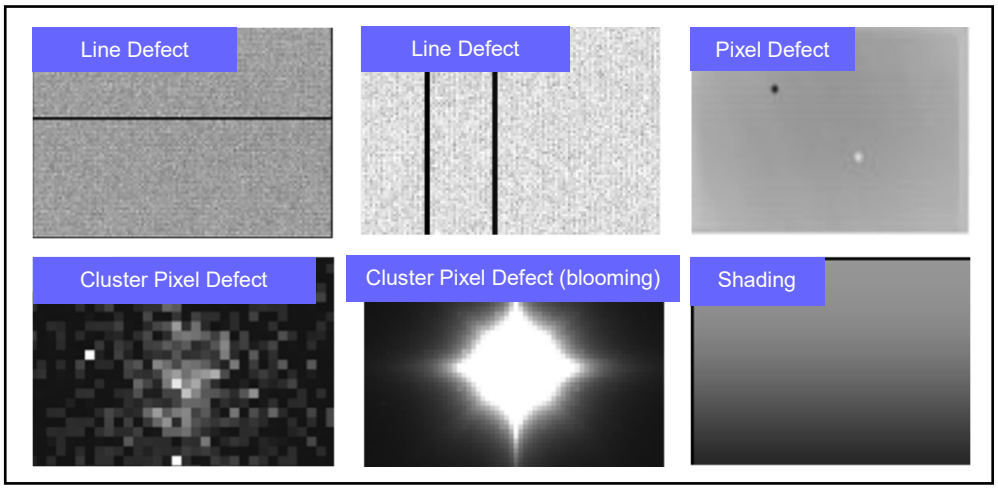


Figure 5-4 Photographs indicating typical image failures

(2) AC and DC characteristics evaluation

If any abnormality is detected according to analysis with a tester, DC characteristics such as open connections, short circuits and withstand voltage deterioration are investigated with using a tool such as a curve tracer and a parameter analyzer.

An oscilloscope is used for simple AC characteristics evaluation to analyze the operating state.

(3) Design For Testability (DFT) analysis

As semiconductors become more miniaturized and their structures become more complicated, a failure location cannot be identified easily with the conventional analysis methods in many cases. By adding the circuit design that allows DFE to narrow down a failure location easily in the design stage, the estimated failure locations are extracted at the circuit level based on the test results and failure simulation.

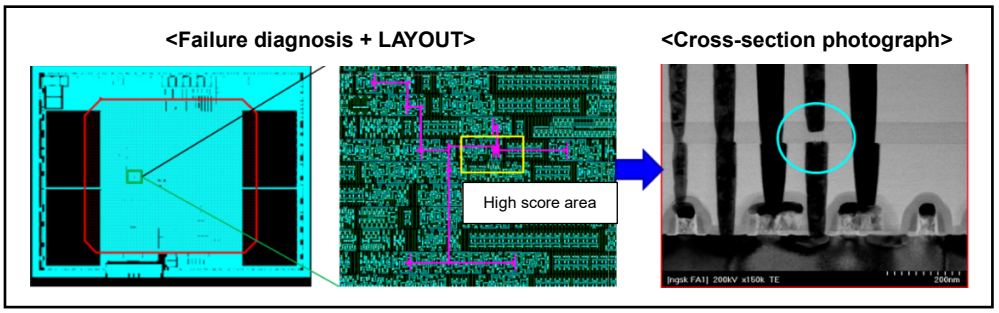


Figure 5-5 Example of identification of a failure location based on the failure diagnosis

(4) Evaluation with using actual equipment

If it is difficult to check the failure state with a tester or the DC analysis, a device that uses laser whose spot diameter is decreased to heat a local position and observes changes in a resistance value or an optical analysis device that detects feeble light emission occurred at a failure location of a semiconductor is linked with the tester or the DC analysis under the condition where the failure is reproduced with the tester or the actual equipment. Narrowing down of a failure start position, visualization of the activated state of the circuit and/or observation of the internal waveform of the device in this condition allow a location causing the failure such as an unstable failure depending on the temperature and a failure very difficult to be detected to be narrowed down.

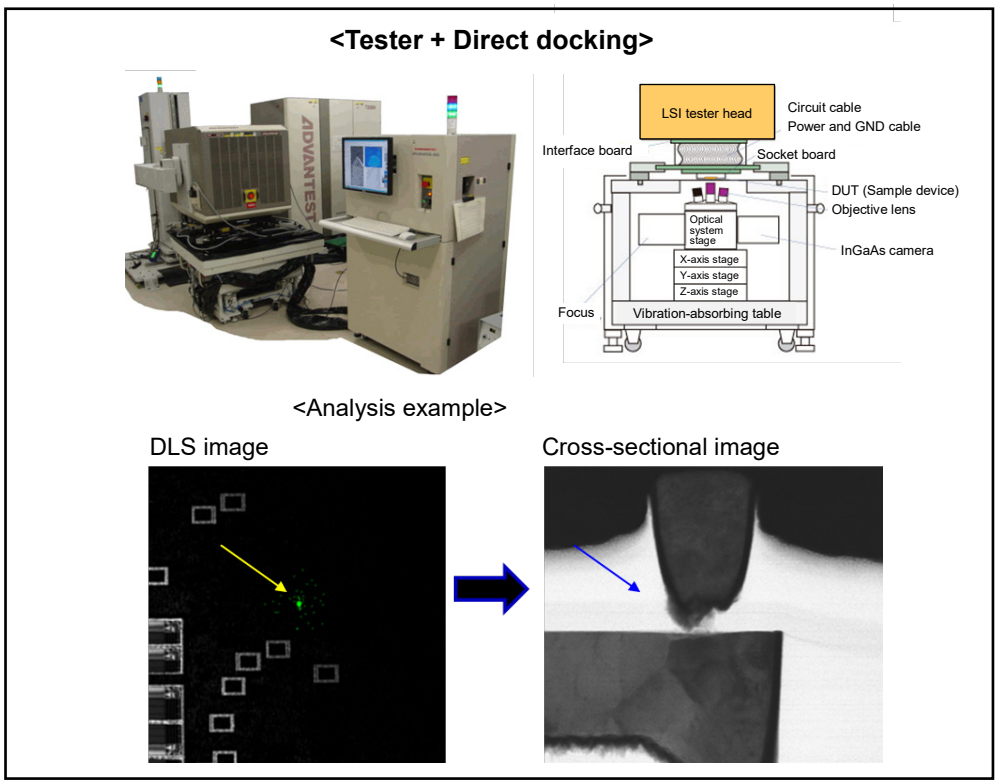


Figure 5-6 Analysis linked with a tester and example

5.3.6 Package/Module Analysis Technology

5.3.6.1 Overview

Building highly advanced functions into a small and thin package/module is required for semiconductor products. As smartphones become thinner, camera modules to be incorporated into them are requested to be thinner. Therefore, we have thinned our camera modules by laminating chips. To analyze a failure, it is necessary to clarify whether the failure occurred inside a chip or it is rooted in the assembly before starting failure analysis.

In addition to such a difficulty of analysis, for example, even a chip in the middle of the 3-layer structure has to be separated without being damaged for analysis. Multilayering and thinning make the analyses more difficult than ever, and each type of microfabrication technology becomes more important under this circumstance. Since the destructive analysis cannot restore the state of a malfunctioning device, we use non-destructive analysis technologies wherever possible. The technologies we use frequently are described below.

5.3.6.2 X-ray Analysis and Scanning Acoustic Tomograph (SAT) Analysis

X-ray inspection allows non-destructive inspection of the wire bonding condition (such as wire loop condition, bump condition and stitch shape), lead frame condition, voids in the molded resin, (the board wiring) and through-hole condition, and micro-bump condition. (See Figure 5-7.)

Since the 3D CT function is enhanced, the internal structure can be checked in three dimensions nondestructively. This is an effective device for estimating the failure mechanism.

Scanning Acoustic Tomography (SAT) or Scanning Acoustic Microscope (SAM) uses the principle that ultrasonic waves are reflected at the bonding interface between materials with different acoustic impedance to make it possible to catch reflected waves of ultrasonic waves oscillated to a sample and to nondestructively observe package internal conditions at arbitrary depths such as separation of bonding interface, voids in the package resin, cracks, and chip cracking. (See Figure 5-8.)

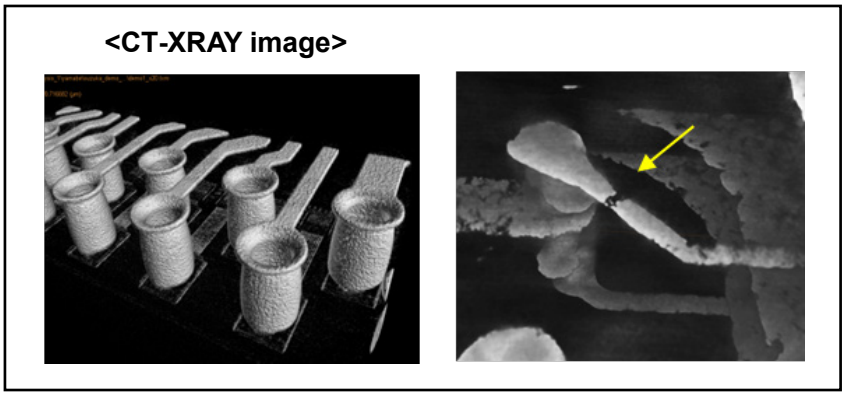


Figure 5-7 X-ray Analysis example

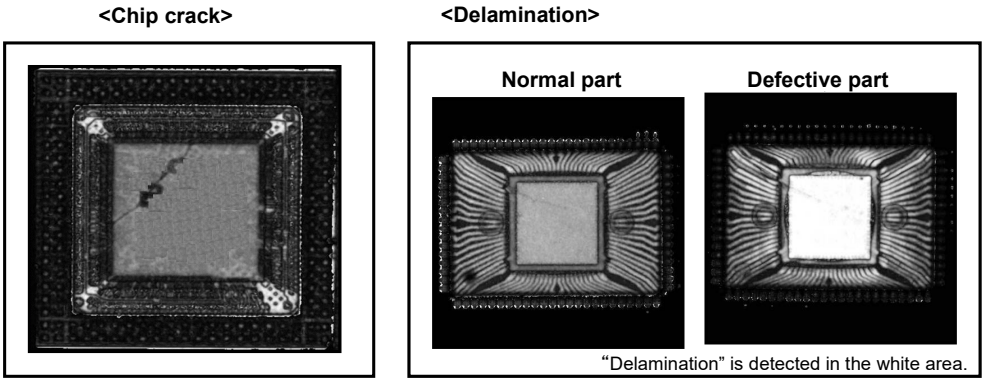


Figure 5-8 SAT Analysis example

5.3.6.3 Scanning Superconducting Quantum Interface Device (SQUID) Microscopic Analysis

SQUID indicates an ultra-sensitive magnetic sensor that uses the superconducting quantization phenomenon. SQUID has far greater sensitivity than conventional magnetic sensors, and can detect weak magnetic fields on the order of 1/50,000,000 of terrestrial magnetism or less. As you know, a magnetic field is generated around flowing current (See Figure 5-9). As described above, SQUID uses an ultra-sensitive magnetic sensor, so it can detect magnetic fields generated by currents. The currents flowing inside a semiconductor device can be observed by using the obtained magnetic field distribution information to create images of the currents that generate the magnetic field distribution. (See Figure 5-10.)

In addition, magnetism passes through almost all materials such as silicon used in semiconductor devices and packages, so current paths can be observed in a non-destructive manner, which is a merit for failure analysis. However, due to the nature of the principle that current paths are shown by detecting magnetic fields, failure analysis using this equipment is valid only in the DC measurement condition where the current direction is constant. Actual failure analysis is performed by first comparing the observed current paths of a good product and that of a failed product to narrow down what caused the failure, and then performing

detailed analysis to identify the cause. An example of analysis using this method is shown below. (See Figure 5-11.)

These results also allow us to identify failure caused due to a minute conductive foreign substance that cannot be easily discovered by X-ray fluoroscopic observation.

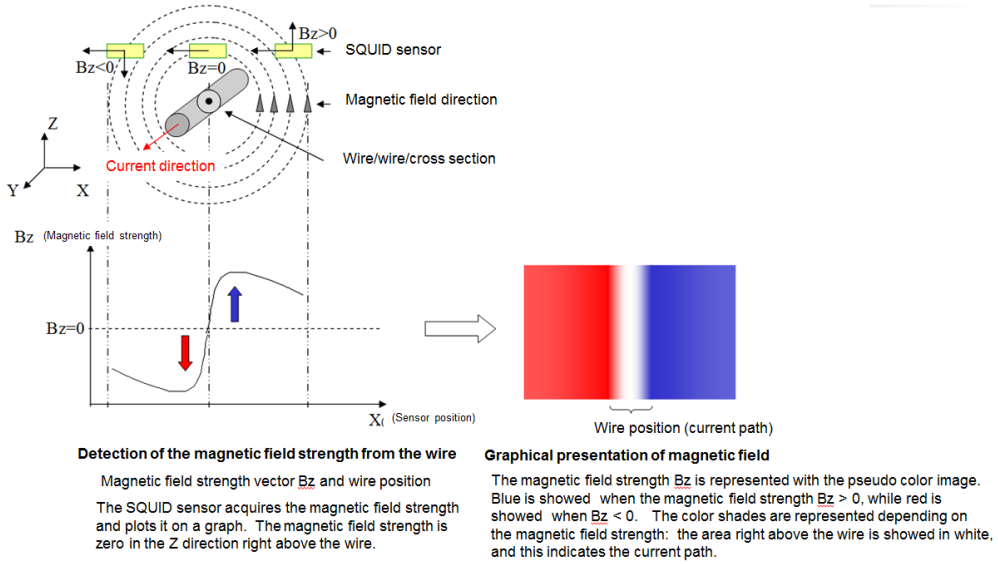


Figure 5-9 Scanning SQUID – Graphic representation of current and magnetic field

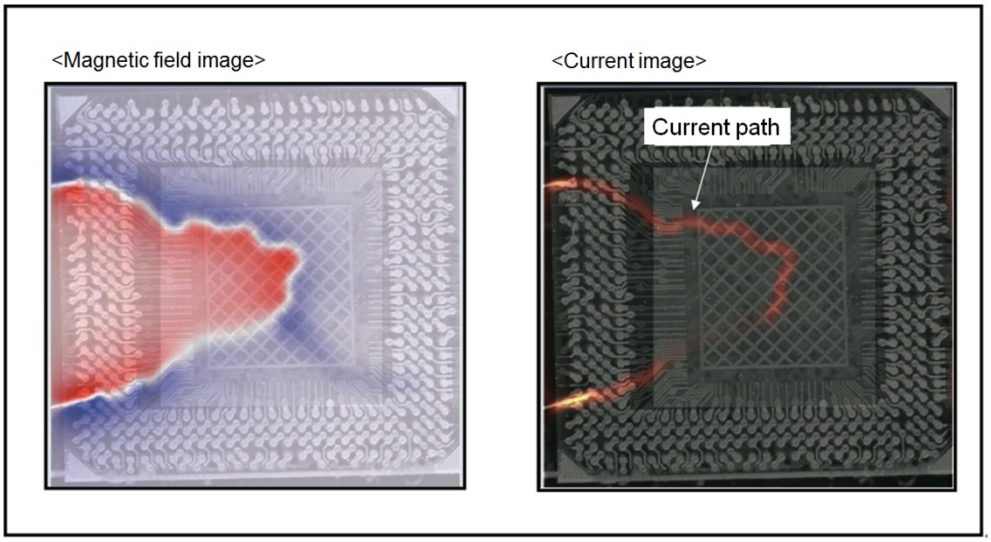


Figure 5-10 Scanning SQUID – Magnetic field image and current image

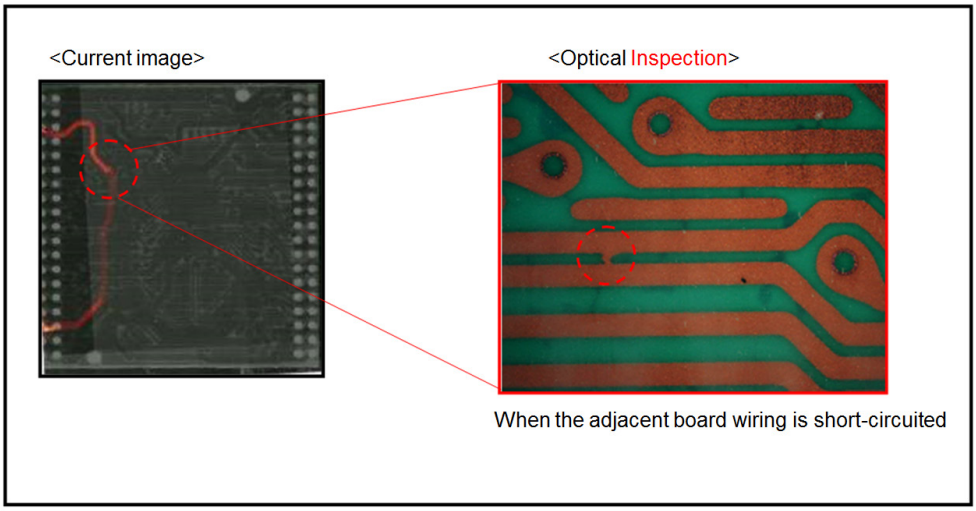


Figure 5-11 Example of using scanning SQUID to identify a failure location

5.3.6.4 Time Domain Reflectometry (TDR) Analysis

TDR is a technique that measures the transmission state of a measuring object by inputting a high-speed pulse signal to the measuring object and observing the reflected signal. This method has been conventionally used to discover disconnection of power transmission lines and other failures. (See Figure 5-12.)

This technique is applied to semiconductor package analysis: a probe is connected to the package electrode estimated to be a failure location, a high-speed pulse signal is applied to the sample, and a sampling oscilloscope is used to observe the reflected waves generated at a location where impedance mismatching of materials is detected. If any open failure such as disconnection of the wiring path occurs, the impedance mismatch increases at the failure location. This generates a large reflected wave. As a result, the waveform of the good product becomes different from that of the defective product. The failure location can be estimated from this reflected wave difference. Although this method can also be applied to determine short-circuit locations in principle, currently it is mainly used to identify open locations.

In the same manner as the SQUID analysis described above, TDR also enables non-destructive analysis, and since there is not any other methods at present that can swiftly determine especially open locations in a non-destructive manner, it is an extremely effective analysis method for analyzing semiconductor device packages. In particular, substrate used in highly functionalized products are multilayered, so overlapping wiring and other influences make it difficult to determine a failure simply with using X-ray fluoroscopic observation. Therefore, failure locations are first reliably narrowed down using TDR, and then X-ray fluoroscopic observation and other analysis methods are performed.

An example of analysis using this technique is shown below. (See Figure 5-13)

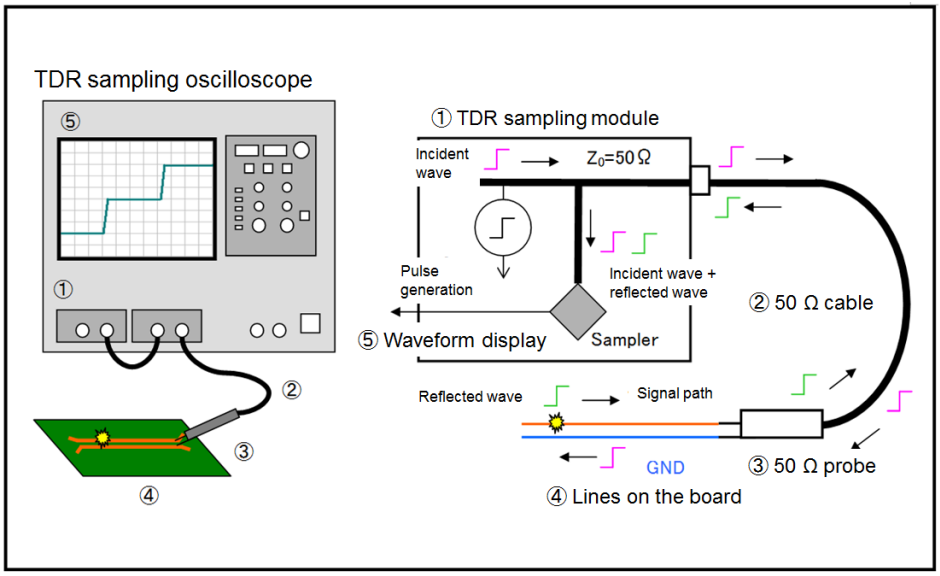


Figure 5-12 General principle of TDR

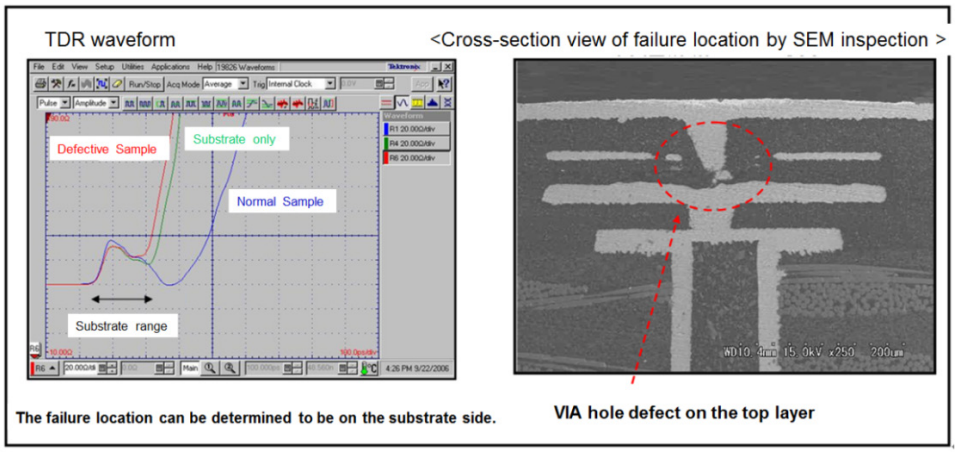


Figure 5-13 Example of a failure location identification with TDR

5.3.6.5 Thermal Emission Analysis

This is a method for identifying a location where heat is generated due to a short-circuited wiring, current leak or resistance abnormality of a semiconductor device. When voltage is applied to a device, heat is generated from the inside of the device. The generated heat is transmitted to the device surface, and the infrared ray emitted from the device surface is observed with a camera. As an infrared camera, mainly a sensor whose wavelength bandwidth is 4.0 μm such as InSb (indium antimonide) and MCT (HgCdTe: mercury cadmium telluride) is used.

OBIRCH or emission analysis can be used also as a method for identifying a current leak location. However, this heat generation analysis can narrow down a failure location of a package covered with a mold, a laminated device, a module state or a printed wiring board nondestructively without taking out a semiconductor chip supposed to cause a failure or without exposing it because this analysis observes infrared radiation caused by heat. (See Figure 5-14.)

On the other hand, the wavelength bandwidth of the sensor is on the long wavelength side, so this analysis is inferior to OBIRCH or emission analysis in spatial resolution. According to a failure symptom, it is important to narrow down a failure location with combining this heat generation analysis with another method. In addition, since it is difficult to detect a failure location when a material whose emissivity is low such as metal is located on the surface, it is necessary to devise a unique method, for example, removal of the metal or application of a material for raising emissivity to the surface.

The method using a lock-in amplifier supplements a defect that the spatial resolution is inferior: this method reduces diffusion of heat, and eliminates external noise to allow highly sensitive analysis. The time for transmitting the heat generated inside a device changes depending on the distance to the chip surface. It is, therefore, possible to estimate a failure location in the depth direction with using this heat generation phase difference.

<Thermal emission analysis image>

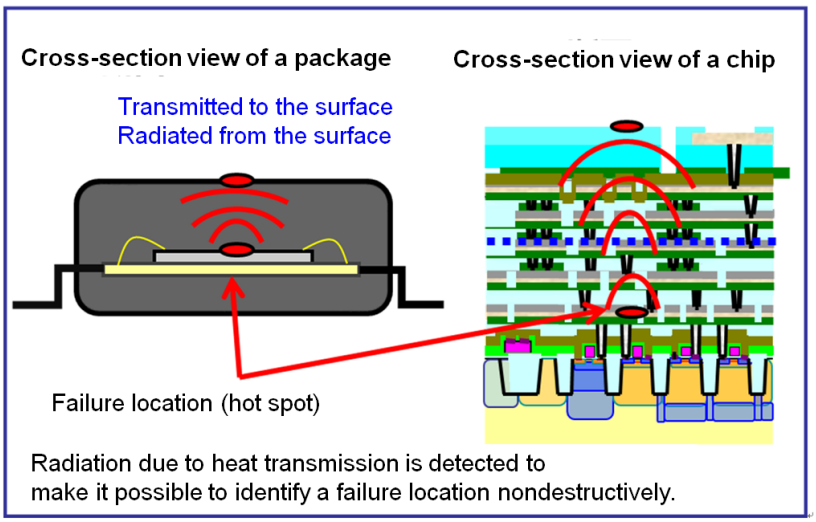


Figure 5-14 General principle of heat generation analysis

5.3.7 Chip Analysis Technology

5.3.7.1 Overview

As described above, products have become more highly integrated and more functions have been incorporated into them in recent years. As a result, circuits are also increasing vastly in both scale (several ten to hundred million gates) and complexity, which means that it is not an easy task to narrow down the locations of failures in a range within several μm and investigate the causes. To analyze a failure of a chip, several analysis methods have to be combined such as failure inference technology using software in addition to emission analysis, heat generation analysis, IR-OBIRCH (Infrared-Optical Beam Inducted Resistance Change), Dynamic Laser Stimulation (DLS), micro-probing technique. As chips are laminated and thinned, the processing technique for taking out only a chip to be analyzed without damaging it becomes one of the important analysis techniques. However, since narrowing down of a failure location becomes complexed and the difficulty of the technique for taking out the narrowed down chip becomes higher, it takes an extremely long time to analyze a failure. Therefore, in addition to improvement of the failure cause determination rate, shortening of the turn-around time (TAT) from start of analysis to end has also come to be an important issue for the current failure analysis technology.

The main analysis methods used to determine failure locations in various chips are extracted, and then their roles and functions are described below.

5.3.7.2 Fail Site Isolation Technology

Mechanical probing technique, electron beam (EB) testing technique, emission analysis technique, heat generation analysis technique and other techniques are widely known as conventional techniques for identifying failure locations inside chips. Semiconductor devices have become more miniaturized, highly integrated, and multi-functional, and have speeded up in recent years. As a result, failures cannot be found by using only one of these analysis methods in many cases, so it has been necessary to use multiple analysis methods including even newer methods to narrow down and pinpoint failure locations. However, since the combination of methods used to narrow down the failure location must be always determined based on information obtained when the electrical characteristics are checked, it is difficult to provide a specific written rule. Methods often used for failure analysis and the latest techniques are described below, focusing on the applications and information that can be obtained by each technique when it is used alone.

5.3.7.2.1 Failt Simulation Technique

Recently, due to increases in logic circuit scales, the difficulty level of electrical analysis of circuits has become noticeably higher than ever. This is because most parts are configured of complicated digital logic circuits, there is no clue about which part malfunctions, and it is extremely difficult to narrow down a failure location. As for this problem, a failure can be identified by mounting a circuit dedicated for testing on a product in the chip designing stage in order to test the function of the product itself easily, and inferring a failure (failure simulation) even when a failure occurs actually. As the failure inference mechanism, by preparing various failure models in the database from the circuit dedicated for testing mounted on a chip as the start point, the test itself can be performed without omission, and which circuit caused a failure can be estimated if it occurs. (See Figure 5-15.)

When the area in which a failure may have located is narrowed down further by another analysis method based on this inference results, the identification rate of a physical failure location is improved drastically. A method for analyzing a failure related to delay, which frequently occurs due to process miniaturization, has been developed by the recent failure inference technique, and this technique becomes necessary for investigating the cause of a failure case having a high degree of difficulty.

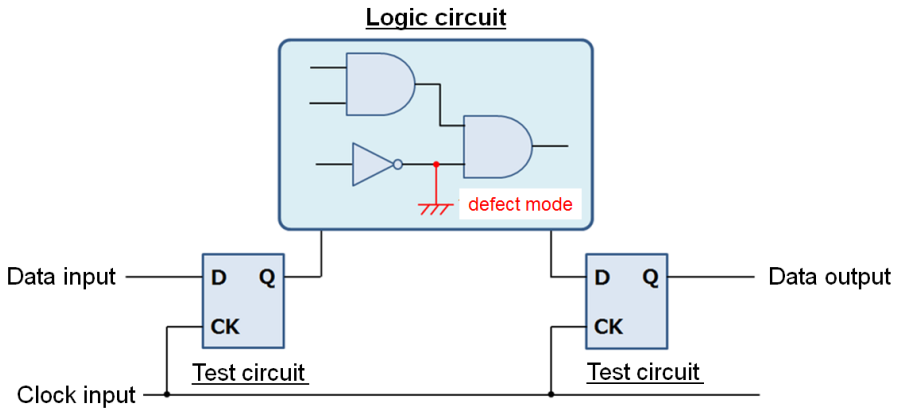


Figure 5-15 General fault simulation model

5.3.7.2.2 Photo Emission Analysis Technique

Photo emission analysis is a well-known method for analyzing current leaks in semiconductor devices.

Current leaks generally involve extremely weak light emissions produced by hot electrons and reuniting of minority carriers. In addition, since the current flows also in case of through-current flow caused by latch-up or intermediate potential or in case of normal transistor operation, light is emitted. This method narrows down failure locations by detecting these light emissions with using a super high-sensitivity cooling CCD camera (effective sensitivity: approximately 200 nm to 1000 nm) and creating images of the semiconductor device circuit location where the light is emitted. (See Figure 5-16.)

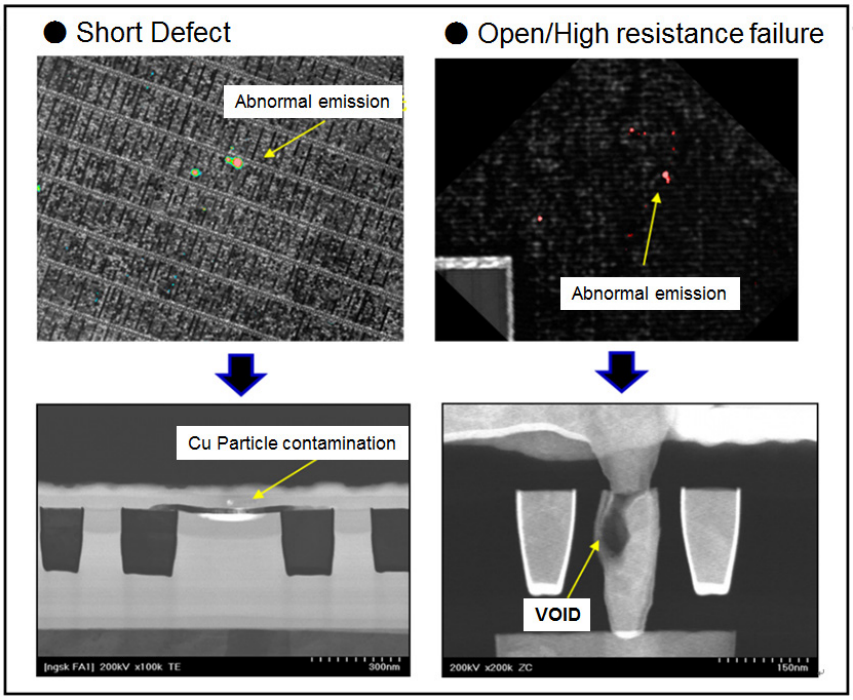


Figure 5-16 Light emission analysis example

Recently, MCT cameras and InGaAs cameras (effective sensitivity: approximately 800 nm to 2000 nm) both of which show the good sensitivity in the infrared wavelength range have been mainly used. Since these cameras have extremely good sensitivity characteristics in the infrared range, they are highly effective at capturing light missions from the rear side of a chip. This method is used to analyze highly integrated and multilayer wiring semiconductor devices by observing infrared light transmitted through the silicon from the rear side of the chip.

In addition, InGaAs cameras are often misunderstood as having higher sensitivity than cooling CCD cameras generally, but the wavelength band captured by each camera type is different from each other. Therefore, it cannot be absolutely said which type has the higher sensitivity than the other. However, since silicon is mainly used as the material surrounding transistors, InGaAs cameras with extremely good sensitivity for infrared light that easily passes through silicon are advantageous for analysis of recent semiconductor devices. (See Figure 5-17.)

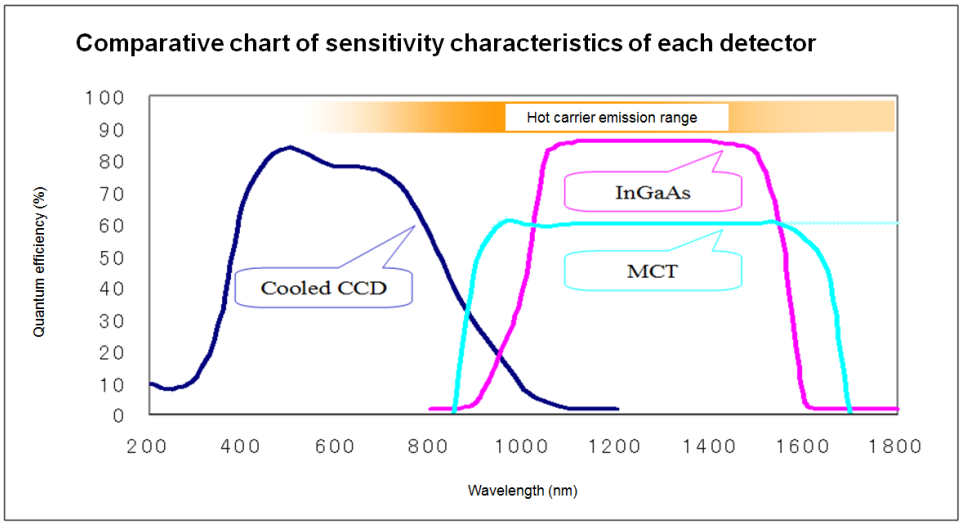


Figure 5-17 Photo emission sensitivity characteristics of each detector

One merit of the emission analysis method is that analysis can be performed in either the AC state or the DC state. However, since current flow involves some light emission, the meaning of light emission captured by light emission analysis has to be examined closely and interpreted. All light emitting locations are not necessarily failure locations. Therefore, it is important to not only rely on light mission analysis, but also combine multiple analysis methods so that comprehensive judgment can be made to narrow down failure locations. (See Figure 5-18.)

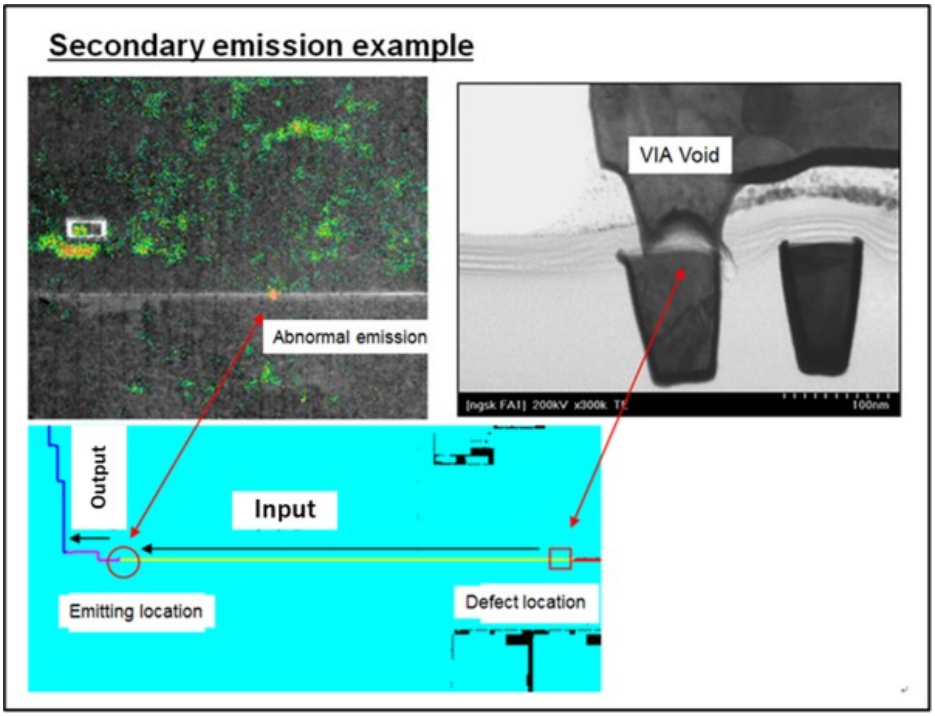


Figure 5-18 Example: A failure did not occur at the light emitting position.

5.3.7.2.3 Thermal Emission Analysis Technique

Heat generation analysis is applied to chip analysis also. This analysis is used together with another analysis such as light emission analysis described above to contribute to narrowing down of a failure location. The details are described in Section 5.3.6.5.

5.3.7.2.4 IR-OBIRCH Analysis Technique

This analysis technique follows the principle described below to determine failure locations such as short-circuits between wiring and high-resistance areas

- A near-infrared laser is radiated to partially heat wiring to which a constant voltage is applied.
- The change in temperature causes the wiring resistance to change, then the current flowing through the wiring to change also.
- Failure locations are identified by using a high-sensitivity amplifier to detect this change in current.

As you can see from the principle above, this method detects the current change made when a near-infrared laser is radiated to a failure location. Therefore, unlike the previously described light emission analysis, almost all responding locations are detected as failure locations. However, analysis can be performed only at the DC level, so this method is not appropriate for trouble modes in which a failure cannot be reproduced without using a semiconductor testing device or other tool. Since the near-infrared laser passes through a silicon substrate, the rear side of chips can also be analyzed easily. (See Figure 5-19.)

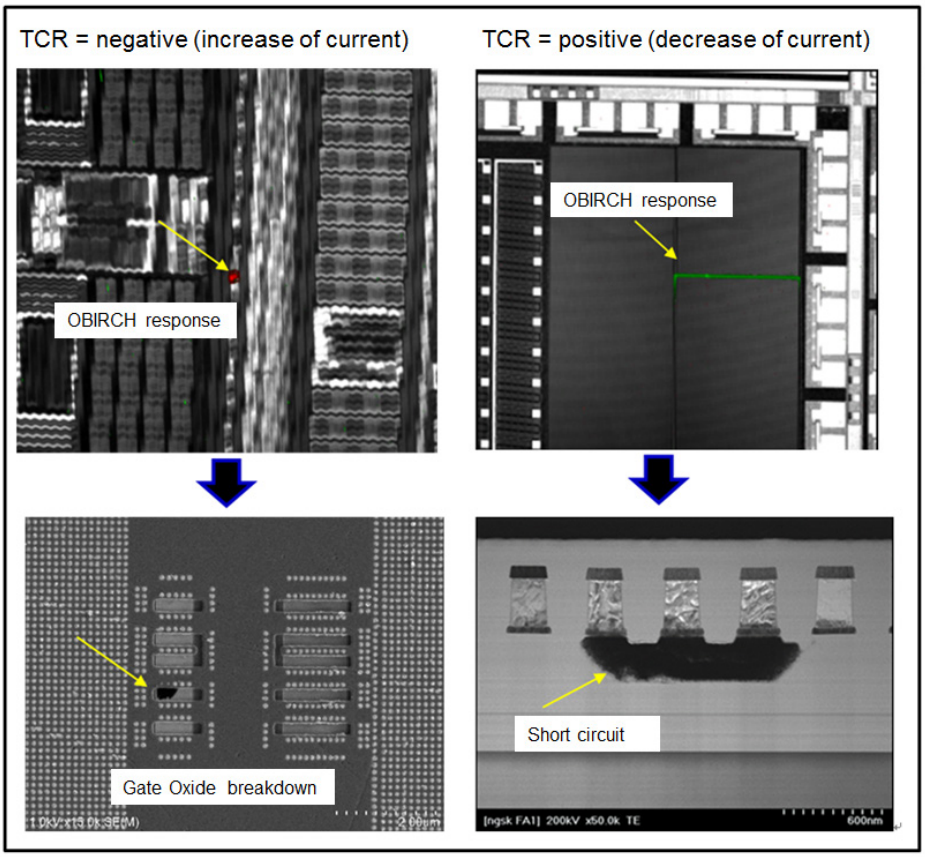


Figure 5-19 IR-OBIRCH analysis example

5.3.7.2.5 Dynamic Laser Stimulation (DLS) Analysis Technique

As semiconductor devices become more miniaturized and faster, the number of defects of margin nature caused due to time delays increases. A defect of margin nature is unstable mode that passes inspection depending on the operating conditions. This makes it difficult to narrow down a failure location by existing analysis methods, and then DLS is gathering attention as an analysis method that can identify such a failure.

The DLS analysis method focuses on the fact that many time delay failures are dependent on the temperature, and makes use of temperature changes caused by local laser radiation. When a device is operated using semiconductor test equipment and an infrared laser whose wavelength is 3.3 μm is radiated to the device from the front or rear side, the temperature of the radiated part changes. As a result, the pass/fail status of the device inverts. When this change in the pass/fail status is read from the semiconductor test equipment and overlaid with the laser image to be displayed, the failure location is identified.

DLS is an effective analysis method for identifying a failure highly dependent on the temperature such as a wiring defect like voids and characteristic abnormality of transistors. On the other hand, since this analysis method also requires the devices to be repeatedly operated for a long time, it has to make the condition settings extremely severe such as temperature control that takes into consideration the heat generated by the device and test parameter settings for the pass/fail status changed by local laser radiation. (See Figure 5-20.)

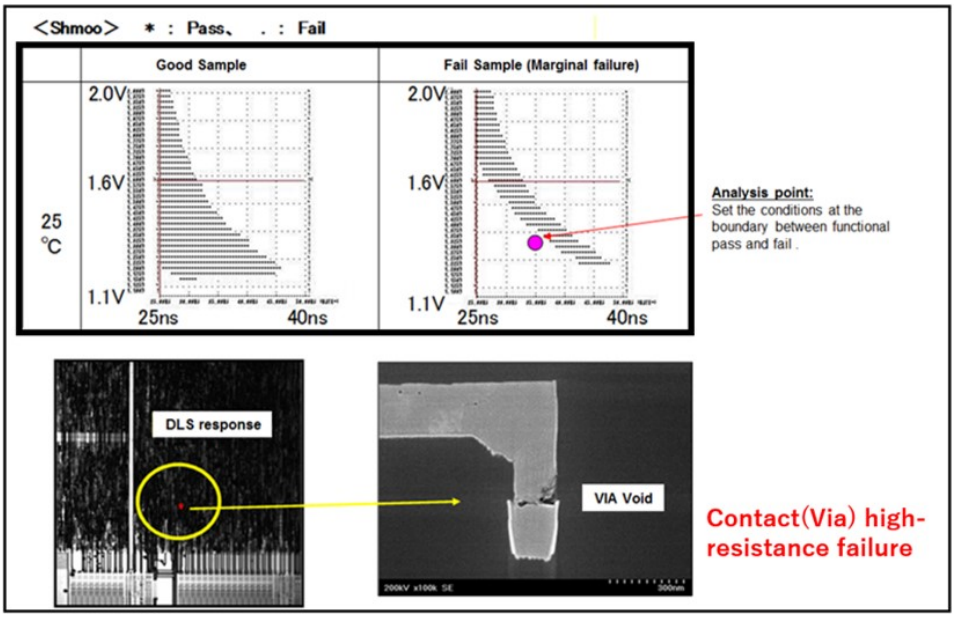


Figure 5-20 DLS analysis example

5.3.7.2.6 Electro Optical Probing (EOP)/Electro Optical Frequency Mapping (EOFM) Analysis Techniques

As a timing analysis method of a device, a method referred to as an “EB tester” has been used conventionally. However, since this method uses an electron beam, the wiring to be observed has to be exposed to the beam.

The recent complication, multi-layering or miniaturization of a device has made processing for exposure of wiring difficult, so this method cannot be applied to identification of a failure location easily.

As a method for responding to this problem, the methods, EOP and EOFM, are provided: these methods radiate a beam of the light source whose wavelength passes through Si from the rear side (silicon side) of the device to perform a timing analysis of the inside of the device. EOP/EOFM radiates incoherent light passing through silicon and detects the reflected light corresponding to operation of the device to observe the internal waveform of a chip nondestructively. (Figure 5-21)

When a transistor operates, the potential near the drain changes, so that the refractive index and the light absorption rate change. The strength and phase of the reflected light of the light source radiated to the device change also (Field optical effect).

The technique for detecting change in the reflected light and corrugating it to observe the actuation waveform inside of the device is EOP. On the other hand, EOFM uses a spectrum analyzer to extract the specified frequency components from the strength waveform of the reflected light and creates a 2-dimensional map to identify the position of an element operating at the certain frequency. This is an effective method for visualizing an element operating at the certain frequency, and it is frequently used to identify a failure of a scan chain.

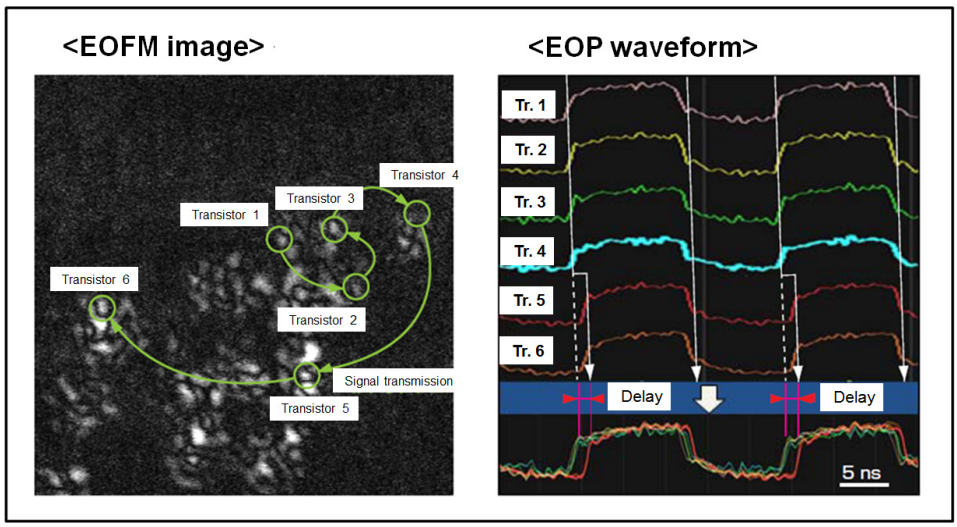


Figure 5-21 EOP/EOFM analysis examples

5.3.7.2.7 Micro Probing Analysis Techniques: Characteristics Evaluation/Electron Beam Absorbed Current (EBAC)

This technique obtains the electrical characteristics by directly probing exposed semiconductor element wiring and contacts with using a microscopic probe. Although conventionally mechanical probing with using an optical image was mainly used, the micro probing techniques described below are now mainly used due to recent miniaturization of semiconductor elements.

① Probing using a scanning electron microscope (SEM) prober

The main probing method is changing from the conventional prober that uses an optical image to a device called a nanoprober that performs probing with inserting a metal probe (into an SEM) while viewing the SEM image. The nanoprober uses a highly accurate probe that can be controlled at the nano level by piezo elements, and a field-emission type electron gun that provides high resolution to enable direct probing of wiring and contacts in the most advanced processes. In addition, the nanoprober can also be used together with electron beam absorbed current (EBAC*) technology by using an electron beam, and this is expected to occupy an important position as a method for identifying a failure location inside a chip. (See Figure 5-22.)

* EBAC is described hereafter.

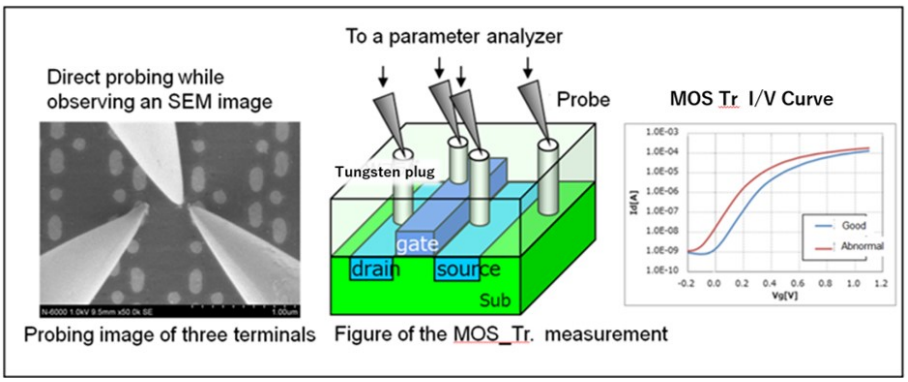


Figure 5-22 Probing example by an SEM type prober

② Probing using an Atomic Force Microscope (AFM)

Devices that scan the sample surface using a probe that is sharp at the atomic level and measure surface shapes and electron states at the atomic level are collectively referred to as scanning probe microscopes (SPM), and there are various types of SPMs whose types are to be selected according to the close interaction of a target to be detected. Atomic force microscopes (AFM) use a microscopic flat spring called a cantilever as the probe, and scan the sample while making contact with its surface. The cantilever displacement caused with the sample surface condition is detected to obtain an AFM image. In addition to the previously described SEM prober, we also currently have an AFM prober, and can obtain the electrical characteristics of elements by probing wiring and contacts with the cantilever based on the acquired AFM image. This is used to evaluate the characteristics of analog products in particular. (See Figure 5-23.)

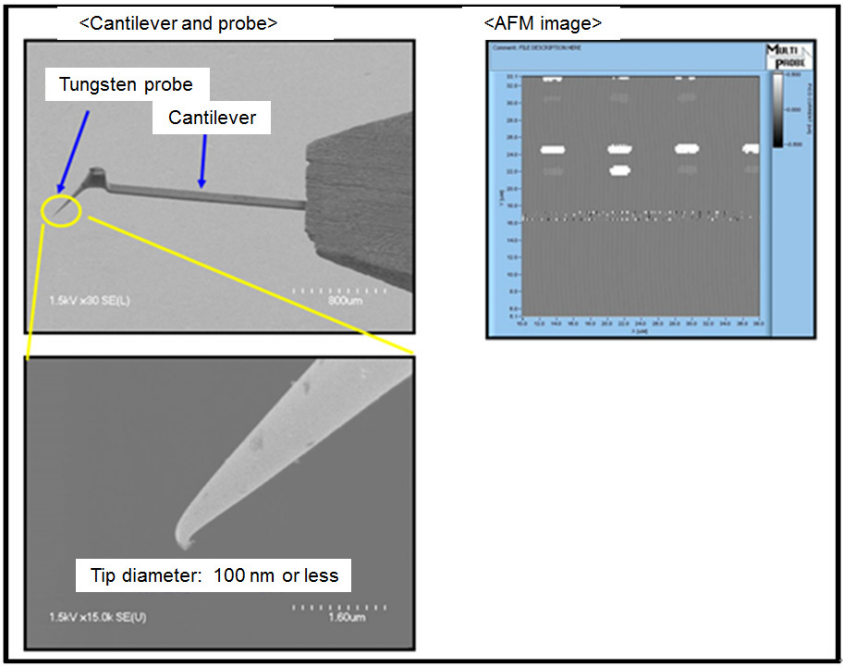


Figure 5-23 AFM prober example

③ EBAC technique

As semiconductor device elements become more miniaturized or multi-layered wiring, the more failures are caused by the wiring via holes that connect each layer. In addition, wiring via hole defects are difficult to be narrowed down by existing analysis methods such as emissions analysis and IR-OBIRCH, and often cannot be checked by two-dimensional observation with using layer removal analysis. Then, effective analysis methods are required.

EBAC is an effective analysis method for the wiring via hole open connection or high resistance failures described above, and radiates an electron beam to a device and uses the current absorbed by the metal wiring (= absorbed current). The principle of the equipment is as follows: the equipment radiates an electron beam to a subject device while directly probing a specific wiring or contact with a highly accurate mechanical probe that uses an SEM prober. The generated absorbed current passes through the probe and then it is amplified by an amplifier, and the equipotential path is displayed as the absorbed current image. When a wire is broken or there is a high-resistance location, light-dark contrast appears in the absorbed current image with this location as the border, and this allows a failure location to be identified. (See Figure 5-24.) In principle, the higher the resistance becomes, the higher the detection sensitivity becomes. Improvement of probing methods and amplifiers enables detection of even low-resistance failures around 100 Ω at the present. The electron beam diameter expands and the spatial resolution is lowered as the beam injection depth increases. Therefore, the practical EBAC analysis depth is two to three layers from the uppermost layer, and analysis of the lower layers requires removal of the upper layers. Performing alternately EBAC and layer removal analysis in this manner establishes an analysis method that identifies failure locations by a combination of electrical and physical analysis.

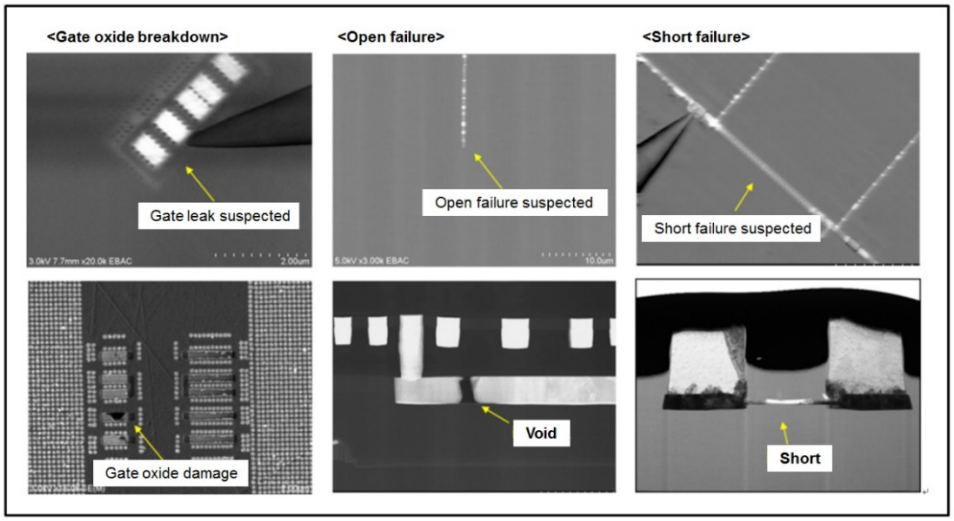


Figure 5-24 EBAC analysis example

5.3.7.3 Special Processing Techniques

To use the failure location identification techniques (see Sections 5.3.7.2.1 to 5.3.7.2.1.7) to narrow down a failure location, we have to electrically reproduce a failure symptom, for example, by operating a device or biasing the abnormal current path. When another chip or package is located in a layer above a chip to be analyzed, it prevents analysis, so the chip has to be exposed.

In this way, the processing techniques for enabling a device to operate and those for exposing a chip to be analyzed are very important to identify a failure location.

5.3.7.3.1 Reassembling Techniques

When a sample for analysis is in a state of a chip, the requirements for applying voltage to a terminal are restricted. Therefore, only simple voltage application can be performed, so that the failure condition cannot be reproduced in some cases, and then a package has to be assembled to analyze the operation. When a failure occurs at an end user's site, the corresponding camera module on which an image sensor is mounted is returned to us. In such a case, the reassembling technique is required to take out the image sensor from the module, and package it so that an electrical test can be conducted. These techniques allow the chip to be taken out without damaging it and to be mounted and wired on a substrate prepared for analysis, so that an electrical test can be conducted easily to reproduce the failure symptom and to analyze the operation.

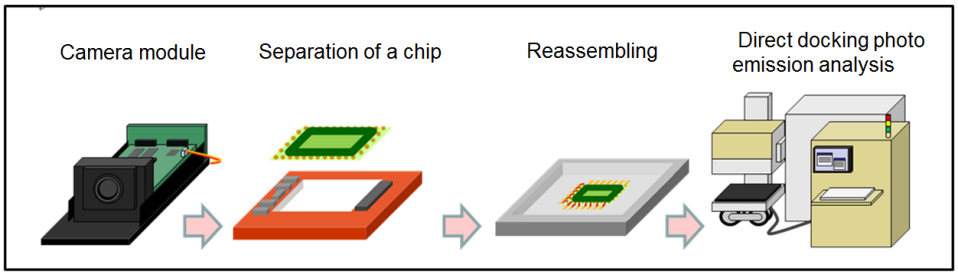


Figure 5-25 Example of reassembling

5.3.7.3.2 Technique for analyzing electrically-alive devices

Due to lamination of wiring layers, the wiring layer prevents analyses such as the light emission analysis from being applied to a device from the top layer. The rear side of a chip, therefore, has to be exposed to be analyzed. Our image sensor cannot be analyzed unless it is opened for us to reach the failure chip due to stacked chips. Therefore, the precise processing technique.i.e.cutting,milling is required to open the rear side of the target chip while maintaining the electrical characteristics. We use the highly precise cutting machine to open the top layer of a chip to expose the rear side of the target chip. This processing requires the electrically activated condition, so it is called “electrically active processing.” This processing technique is very important to investigate the cause of a failure when it occurs at our image sensor.

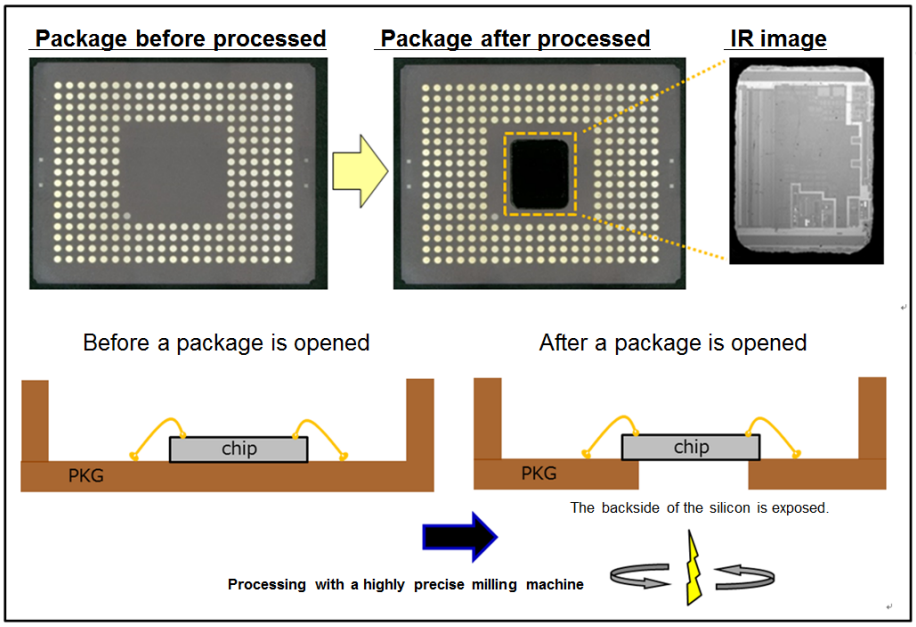


Figure 5-26 Electrically active processing example

5.3.8 Chip Physical Analysis Technology

5.3.8.1 Overview

In semiconductor device failure analysis, various analysis methods are used to narrow down the failure location, and then finally this chip physical analysis technology is used to directly observe the failure location. If observation of a failure location fails at this point although enough time is taken to narrow down a failure location, no information can be obtained eventually, so this is extremely important technology. However, causes of failures such as adherence of a foreign material and pattern corruption are detected in some cases, while failures are not found in other cases even though physical analysis is performed.

Cases where failures are not found are supposed to mainly include the following:

1) Cases in which the failure location was not narrowed down sufficiently, and the failure is located at a different position actually.

2) Cases in which the failure location was sufficiently narrowed down, but:

   ① the failure was overlooked during physical analysis.

   ② an improper physical analysis method was selected (the better analysis method of the interlayer delamination analysis and the cross-section analysis was not selected), so the failure was not observed sufficiently.

In either case, the cause of a failure cannot be investigated only by physical analysis engineers.

It is also extremely important to narrow down a failure location accurately and in the limited area in the narrowing-down stage and to select which analysis method is to be applied after narrowing down a failure location (for example, whether to approach the failure from a plane or from a cross section). These factors affect the failure location identification rate.

In our company, engineers in various fields who are involved in failures always cooperate with one another to improve the failure cause identification rate by narrowing down a failure location, selecting the optimum methods, and finally performing a physical analysis.

The techniques used to perform physical analysis on individual chips are described below.

5.3.8.2 Interlayer Delamination Techniques

To use SEM or other method to physically observe failure locations that are narrowed down with using various analysis methods, the wiring layers and interlayer insulation film that form the circuits have to be delaminated one by one at a time. The typical processing methods for this operation are as follows.

(1) Wet Etching

- Etching is performed for each wiring layer/interlayer insulation film and other items with chemicals.
- Although use of chemicals suited to the materials provides high selectivity, wet etching is isotropic etching (etching progresses in both the vertical and horizontal directions), so it is difficult to apply to microfabrication processing.

(2) Dry Etching

- This etching method uses the physical and chemical reactions between a gas and a solid (the material to be processed). Reactive ion etching (RIE) is a typical method.
- Dry etching is anisotropic etching (etching progresses in only one direction), so microfabrication processing is available.

(3) Surface Polishing

- This method indiscriminately removes all kinds of materials with using a surface polishing machine and abrasives without selecting the target, and the sample surface can be finished to be flat.

Since the latest semiconductor devices are manufactured with a flattening process (chemical mechanical polishing: CMP) and/or a copper wiring process, interlayer insulating films are mainly delaminated with using dry etching, and wiring layers are mainly delaminated with using surface polishing.

5.3.8.3 Chip Front and Rear Surface Observation Techniques

As the observation equipment used to actually find failure causes, stereoscopic microscopes, metallographic microscopes, infrared microscopes, electron microscopes and other equipment are used according to the purpose (such as the size of observation object and location to be observed). Stereoscopic microscopes are mainly used to observe the appearance of packages, and metallographic microscopes are mainly used to observe chip surfaces. Since infrared microscopes allows observation through silicon, they are used for observation from the rear side of the chip without delayering, for example, when a protection circuit is suspected to be broken down. Optical microscopes theoretically have submicron level resolution, but actually they are used to observe a failure on a level of several microns. However, unlike electron microscopes, any large-scale apparatus or preprocessing of samples is not required with the optical microscopes, so they are easy to use. As a result, they are used for “pre-observation” before an electron microscope is used when failure analysis is performed.

Stereoscopic microscopes, metallographic microscopes and infrared microscopes are called optical microscopes also because they radiate a sample with light (such as visible light and infrared light) to observe it. In contrast, as the name implies, electron microscopes perform observation by radiating the sample with electrons. The advantage of electron microscopes is the resolution that enables observation of objects at the atomic level. However, it is large and expensive (several hundred thousand to millions of dollars), and requires a special room that is not subject to magnetic fields, vibrations and other interference. Furthermore, some samples require preprocessing or other preparations, so it takes a long time to prepare for observations.

Electron microscopes are mainly classified into the following two types:

1) Scanning electron microscopes (SEM)
2) Transmission electron microscopes (TEM).

SEM to be used for surface observation is described here, and TEM is described in a separate section.

5.3.8.3.1 Scanning Electron Microscope (SEM)

SEM performs observation by radiating samples with an electron beam to gather into a detector reflected electrons and secondary electrons among the generated reflected electrons, secondary electrons and characteristic X-rays and then imaging their information. The reflected electrons can be used to obtain a composition image of the sample, and the secondary electrons can be used to obtain a rugged image of the surface of the sample (See Figure 5-27). When the remaining characteristic X-rays is used, elemental analysis can be carried out by EDX or other means. SEM is mainly used to observe planar delaminated samples. In addition, during observation with SEM, metal objects connected to a GND appear bright, and floating metal objects and insulating film appear dark (see Figure 5-28), so SEM can also be applied to the Voltage Contrast (VC) analysis method. Insulating film (such as SiO_2) is used in materials of semiconductor devices except the wiring materials. So, when the electron beam is radiated continuously for a long time during observation, the device becomes charged, preventing clear images from being observed and causing burning and other various problems inconvenient to continuation of analysis. Observation should be, therefore, finished quickly in an irreducible minimum time, or charging should be prevented by coating the surface of samples with carbon, gold or other conductive substances in some cases.

<Backscattered electron image of a solder bump> <Secondary electron image of a solder bump>

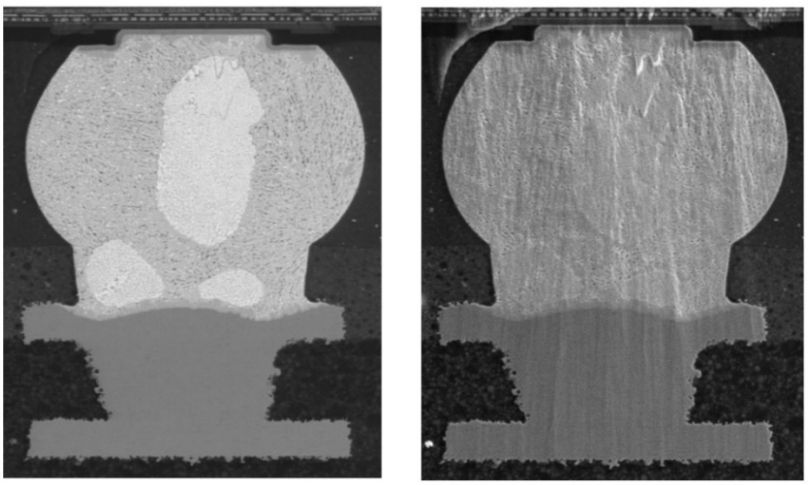
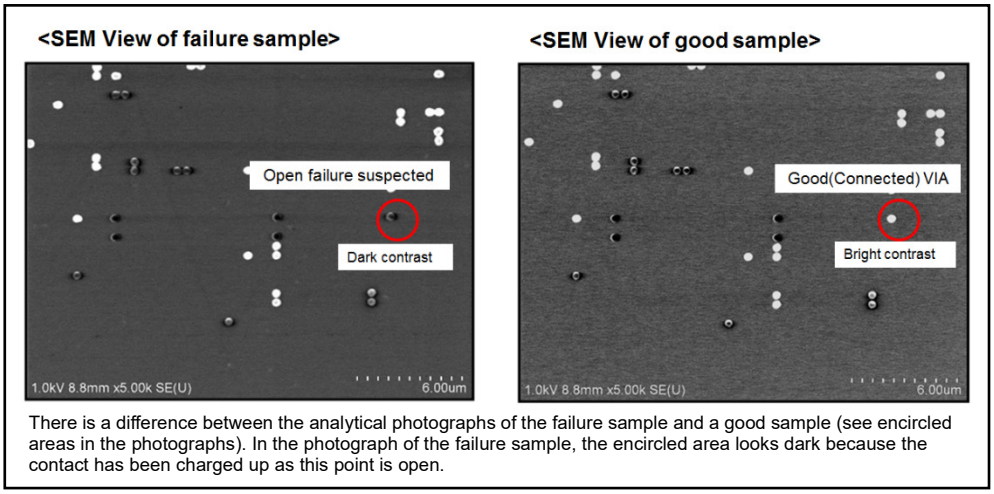


Figure 5-27 Reflected electron image and secondary electron image



There is a difference between the analytical photographs of the failure sample and a good sample (see encircled areas in the photographs). In the photograph of the failure sample, the encircled area looks dark because the contact has been charged up as this point is open.

Figure 5-28 VC method analysis example

5.3.8.4 Cross-sectional Analysis Technique

Cross-section samples for observing the cross-section of a chip are mainly prepared with using FIB. TEM is also used for observing cross-sections of the prepared samples in detail. An area to be observed is sliced thinly with FIB, picked up by a micro-sampling method, and set in a TEM holder, and then the cross-section is observed with TEM in detail. FIB and TEM are described below.

5.3.8.4.1 Focused Ion Beam (FIB)

Gallium (Ga) is mainly used as the ion source, the ions are accelerated by an electric field to create an ion beam, and then this beam is radiated to the surface of the sample. The required area can be etched by ejecting atoms from the surface with the beam. Since the beam can be tightly focused to a diameter of several hundred nm to enable submicron level etching. As another function, FIB can also be used to vapor-deposit conductive films or insulating films. In addition to processing for cross-sectional analysis, this function can be used to repair semiconductor circuit wiring, so that it is possible to create bug-corrected samples of products under development in a short time. A Scanning Ion Microscope (SIM) image can also be observed, and the cross section of a sample being etched or vapor-deposited in the manner described above can be observed easily. In this SIM image, metal wiring connected to a GND appears bright, while floating metal wiring and insulating film appear dark, so this can also be used for the VC analysis method in the same manner as SEM inspection. However, during inspection, the Ga ions constantly hit against the sample surface and etch the inspected location, so inspection must be performed as quickly as possible.

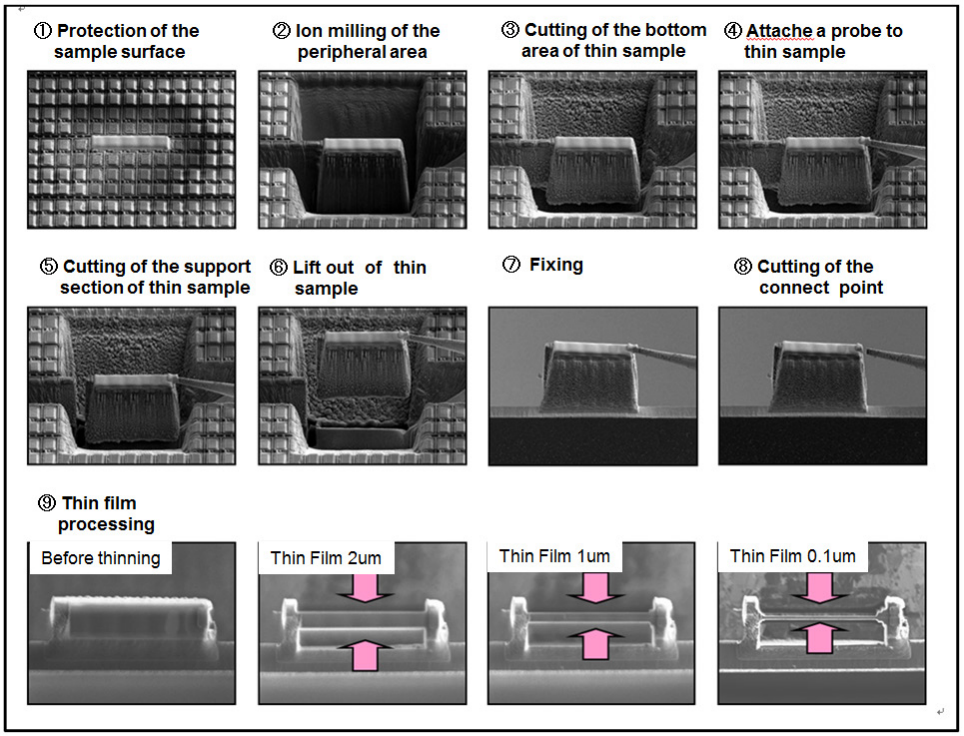


Figure 5-29 Thin film processing example with FIB for observing an object with STEM

5.3.8.4.2 Trancemission Electron Microscope (TEM)

TEM performs observation by radiating a sample with an electron beam, collecting the electrons that pass through the sample with a detector located on the opposite side of the sample, and converting that information into an image. Since the transmission amount of electron beam varies depending on components comprising the sample, information is visualized to observe the sample structure. Therefore, TEM are mainly used to observe cross sections. (See Figure 5-30.)

However, in order for electrons to pass through the sample, accelerated electrons have to be transmitted at an ultra-high voltage (approximately 100 kV to 1000 kV). This means that a large apparatus (total length approximately 2 m to 8 m) is needed to obtain the acceleration voltage, and its installation location is restricted, which is a disadvantage. At the present, samples can be thinned with FIB described above or other device, and technology (Ar milling) for removing layers damaged during FIB processing and finishing a sample is also advancing, so electrons can be transmitted at lower acceleration. Furthermore, Scanning Transmission Electron Microscopes (STEM) that combine both SEM and TEM functions are also used in many cases.

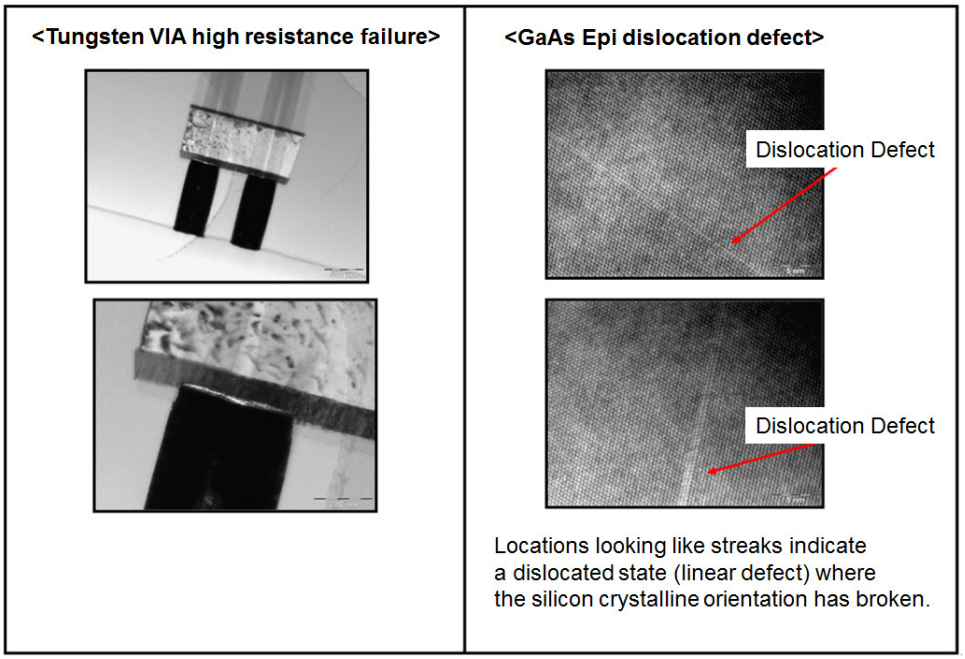


Figure 5-30 TEM analysis example

5.3.9 Material Analysis Technologies

5.3.9.1 Overview

When failure analysis is performed on a semiconductor device, various abnormalities such as adherence of a foreign substance and discoloration of metal wiring materials may be found. Analysis technologies are used to identify these elements and materials, investigate the processes causing the abnormality, and improve these processes.

There are various types of analysis equipment, and the equipment frequently used for failure analysis of semiconductor devices is described below.

5.3.9.2 Fourier Transform Infrared Spectroscopy (FT-IR) Analysis

This analysis method is an analysis method that uses infrared absorption of compound molecules when infrared rays are radiated to a substance and obtains information on bonding state of elements. Since functional groups contained in the measured object are found from the obtained spectrum, this method is used to identify organic substances. Components can be easily determined by comparing with known samples and/or the spectrum in a database. In addition, measurement is performed in the atmosphere, so solids, liquids and gases can be qualitatively and quantitatively analyzed. (See Figure 5-31.)

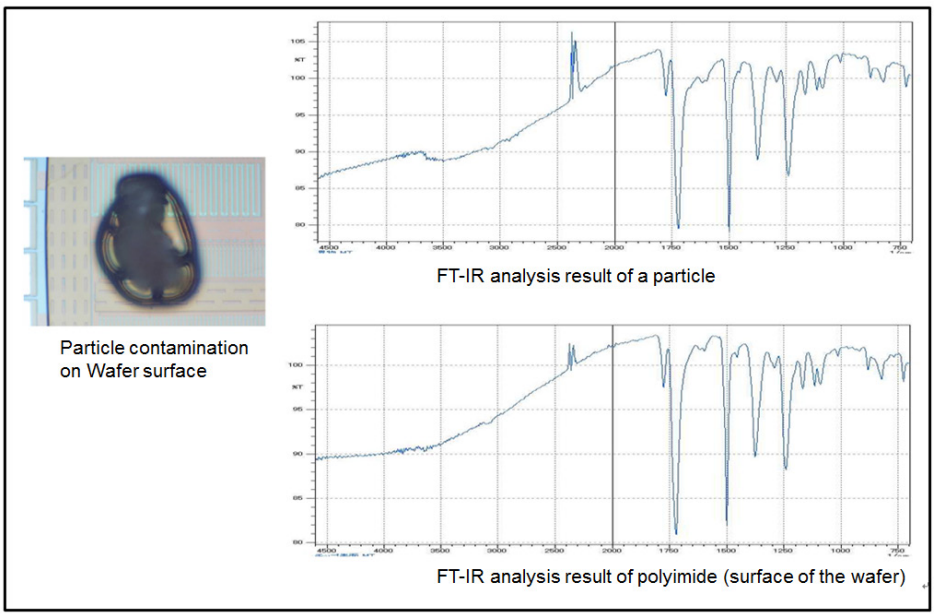


Figure 5-31 Example of analysis with FT-IR

When performing semiconductor device failure analysis, a foreign substance is extremely small. It is, therefore, measured by the microscopic reflection method or the microscopic transmission method with using infrared microscopes. When a foreign substance adheres to metal such as a bonding pad of a chip and a land of a package, the microscopic reflection method is used: the foreign substance can be measured nondestructively. When a foreign substance adheres a substance other than metal such as an organic substrate, the microscopic transmission method is selected: foreign substances are sampled, mounted on a sampling stage whose transmittance for IR rays is high such as a diamond plate and a KBr plate, and then measured. When a substance to be sampled is small, for example, several tens μm, a micro-sampling system is used.

Note that the minimum analysis area for these analysis methods is approximately 15 μm × 15 μm. In addition, the Attenuated Total Reflectance (ATR) method is one of reflection methods too, and this method measures only the surface layer (approximately 1 μm) of a solid. Since this method brings a crystal into contact with the sample, it cannot be used for uneven samples, that is, it can be used for the restricted substances. However, since it is a nondestructive analysis method, it can measure an object while maintaining the failure state. In addition, this method can analyze the surface layer, it can obtain component data on both sides of a substance such as tapes nondestructively. Note that the analyzable area varies depending on the capability of the corresponding equipment, and it is approximately □10 μm to 100 μm.

FT-IR analysis can be performed easily and extensive databases are available. These features make it the most effective method especially for identification of organic compounds. However, the sensitivity is relatively low. It is said that the target has to contain approximately 10 % or more such a compound for detection, and this method is not appropriate for analysis of microscopic areas of several μm or less or minute quantities such as contamination.

5.3.9.3 Energy Dispersive X-ray Spectrometer (EDX) and Wavelength Dispersive X-ray Spectrometer (WDX) Analysis

These analysis methods can identify elements by radiating an extremely tightly focused electron beam to an analysis target (solid) and measuring the characteristic X-rays generated at that time with a detector. In addition, the element quantities contained in the target can also be quantified. Since these methods detect elements to a depth of several microns, they are inappropriate for analysis of the uppermost surface layers. These methods are classified into two types according to the difference in detection methods as follows.

1) EDX (energy dispersion analysis): This analysis method amplifies all of the generated certain X-rays with using a semiconductor detector, and distributes the X-ray wavelengths by energy.

2) WDX (wavelength dispersion analysis): This analysis method uses X-ray dispersive crystals having arbitrarily set wavelengths to select the generated characteristic X-rays and analyze them. Each method has advantages and disadvantages. EDX has the lower wavelength resolution with compared to WDX, but it can analyze multiple elements simultaneously, so qualitative analysis can be performed in a short time. Since the EDX wavelength resolution is inferior to WDX, adjacent peaks often overlap with each other, so the data must be carefully interpreted to avoid erroneous determination. In addition, EDX is not appropriate for analysis of light elements.

   WDX has the better wavelength resolution with compared to EDX, so that adjacent peaks hardly overlap with each other and this method carries a low risk of wrong determination at identification. WDX uses dispersive crystals to measure the target element while changing the angle of the dispersive crystals. It can, therefore, analyze very small amount

of element (approximately 10 ppm), and this method can also detect light elements that cannot be detected by EDX. However, since this method cannot detect two or more elements at the same time, it takes a long time to analyze the element. In addition, in comparison with EDX, WDX requires the larger amount of probe current, and this causes a sample to be damaged much. WDX has also disadvantages.

When performing actual analysis with making use of the characteristics described above, it is common to check the constituent elements with EDX, and perform the detailed analysis with WDX to check to see if the identification results are correct. (See Figures 5-32 and 5-33.)

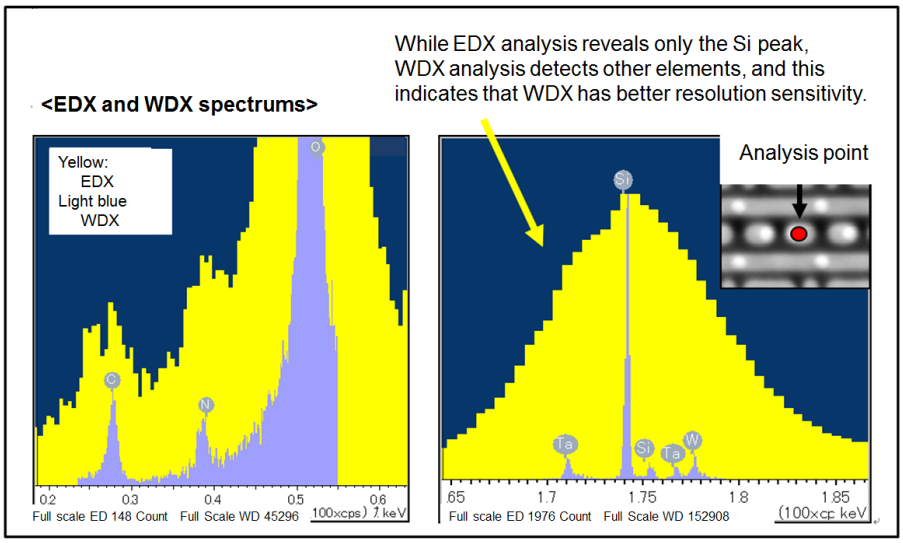


Figure 5-32 EDX/WDX analysis example

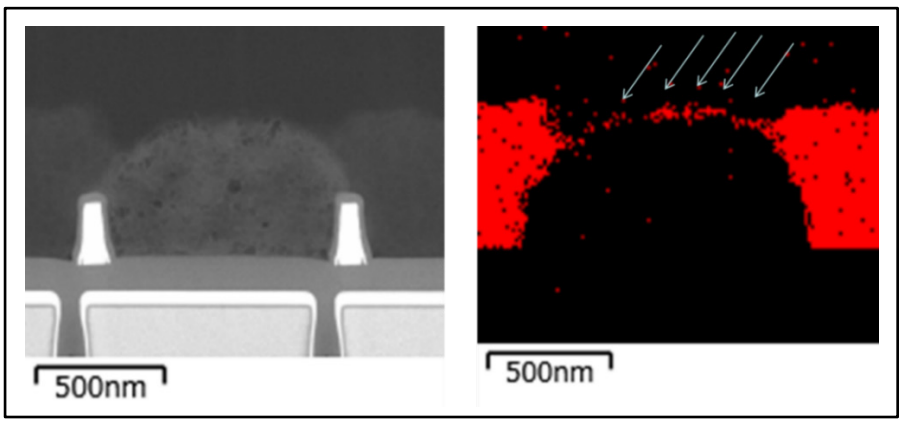


Figure 5-33 STEM cross-section observation (left) and image mapping (right) of a pixel characteristic defective part with EDX/WDX. Although it is not judged with the STEM image, it is clear that another color filter component remains on the corresponding color filter (indicated with arrow marks).

5.3.9.4 Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS) Analysis

The Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS) analysis uses a difference of a flight time (flight time is proportional to the square root of the weight) of the secondary ions emitted from the surface of a solid material due to a sputtering phenomenon when the pulsed primary ion beam is radiated onto the surface to perform mass separation. Since this method highly sensitively detects information on elements or molecular species existing at a depth approximately 1 molecule from the surface of a sample, it is used to analyze the top most surface.

Although a sample has to be treated carefully because this method is subject to effects of the cross-contamination, this method can analyze and identify the structure of an organic/inorganic compound (even analyze an insulator). It, therefore, covers a wide range of samples, and especially it can analyze pollution such as a stain well.

By operating the primary ion beam, this method can also obtain an ion image (imaging) of the surface of a sample. In addition, by repeating etching the surface of a sample with ion sputtering and measurement, this method can analyze the depth too. This allows acquisition of a depth profile or establishment of data to provide a planar or cross-sectional image.

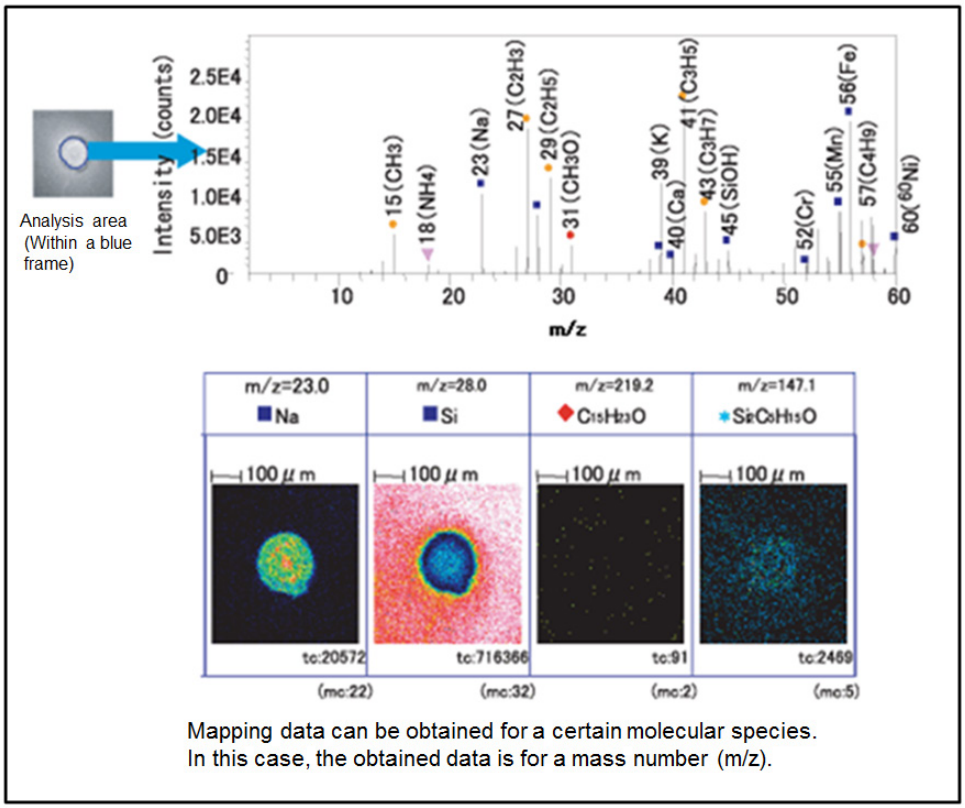


Figure 5-34 TOF-SIMS analysis example

5.3.9.5 Scanning Probe Microscope (SPM)

A scanning probe microscope is a general term for the technology that uses a minute probe such as a Scanning Tunneling Microscope (STM) or an Atomic Force Microscope (AFM) to scan the surface of a sample, and then detect interaction between samples.

This method can measure various items such as a shape, mechanical characteristics and electrical characteristics depending on interaction to be detected, and uses a nano-level minute probe to scan a sample, so its resolutions is atomic-level, and it has an enlargement capability whose level is similar with that of a transmission type electron microscope (TEM).

Although this microscope has high resolution, it does not require vacuum environment unlike SEM or TEM, and can be used in the atmosphere, so that it is used in many fields such as living things, materials and semiconductors.

SPM has characteristics that allow it to visualize dopant by detecting electrical actions between samples. According to a detected electrical action, the following types are known: Scanning Capacitance Microscopy (SCM), Scanning Spread Resistance Microcopy (SSRM), Scanning Microwave Microscopy (SMM). Since many types of dopants are dosed into the sensor area complicatedly in case of our image sensors, the method described above is used as one of failure analysis techniques to visualize dopant.

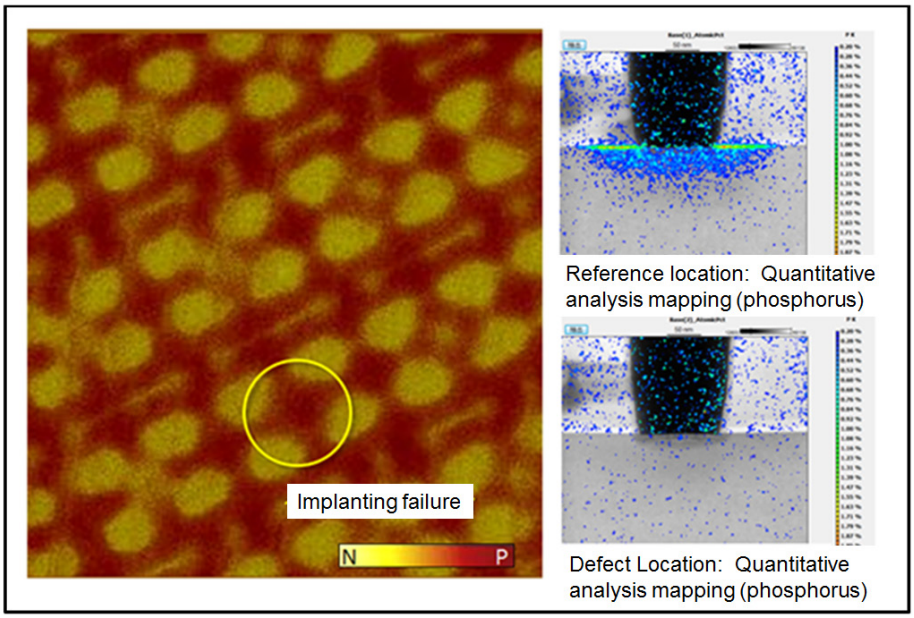


Figure 5-35 SPM analysis example (left) and EDX image map of the cross section (right)

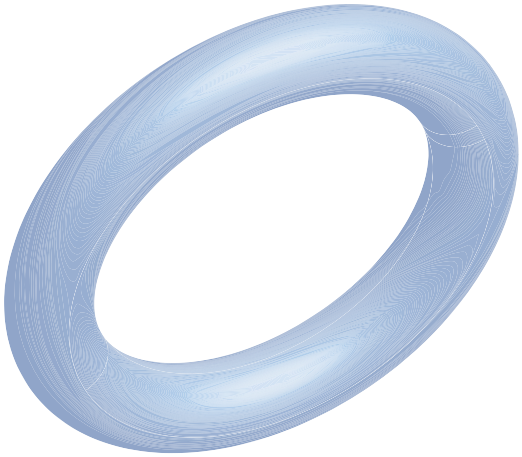
5.3.10 Verification of the Relation between Failures and Malfunctioning Mechanisms

It is important to be able to explain that the “failure” identified when failure analysis is performed caused a device to malfunction based on the supportive evidence. Even though there is a failure, it does not cause the corresponding device to malfunction in some cases.

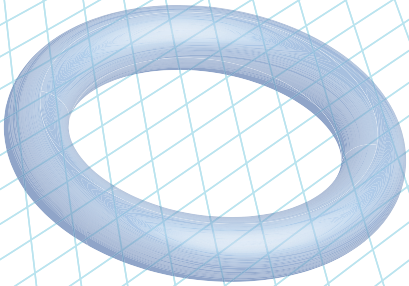
For example, even though shape abnormality is found in a wiring pattern, the wiring pattern does not look good in fact, but it does not cause the device to malfunction unless any wiring is in contact with adjacent wiring. In such a case, there is always some other real cause of the malfunctioning, and the real cause has to be found to lead to proper improvement of the device.

When a failure is confirmed with using various analysis methods in this manner, we have to explain that the failure is not inconsistent with the failure symptoms and electrical characteristics. Only if this can be explained, it can be said that the failure cause is identified. However, as a result of recent increases in semiconductor device integration and circuit scale, failure symptoms have also become more complicated, and this makes it difficult for analysis technology engineers alone to determine whether failure symptoms match failure causes.

In our company, engineers such as engineers of circuit designer, product engineering, reliability engineering, and process engineers all cooperate with one another to reliably investigate failure mechanisms, implement the appropriate improvements, and conduct continuous quality improvement activities.



Chapter 6 Precautions for Handling Semiconductor Devices



Chapter 6 Table of Contents

6.1 Solder Heat Resistance

Because of miniaturization and multifunctionality of electronic products, Surface Mount Devices (referred to as “SMD” hereinafter) have become widely used in recent years, and then the number of pins has increased and the size of packages has been larger also. When handling an SMD, you have to keep in mind the following failure: its package may crack when soldering is performed by using a reflow oven or other method that heats the entire package.

To prevent this problem, we not only improve package composing materials and structures but also rank products according to the package crack resistance (Basically, we adopt JEDEC implementation level (MSL)), and request customers to mount a product on their devices by soldering it based on these ranks.

This section describes the package cracking mechanism, and other notes to prevent a package from cracking in the mounting process. See section 6.4 for the general notes on soldering of semiconductor products.

6.1.1 Package Cracking Mechanism

(1) Package cracking phenomena

A package cracks during mounting through the following process. (See Figure 6-1.)

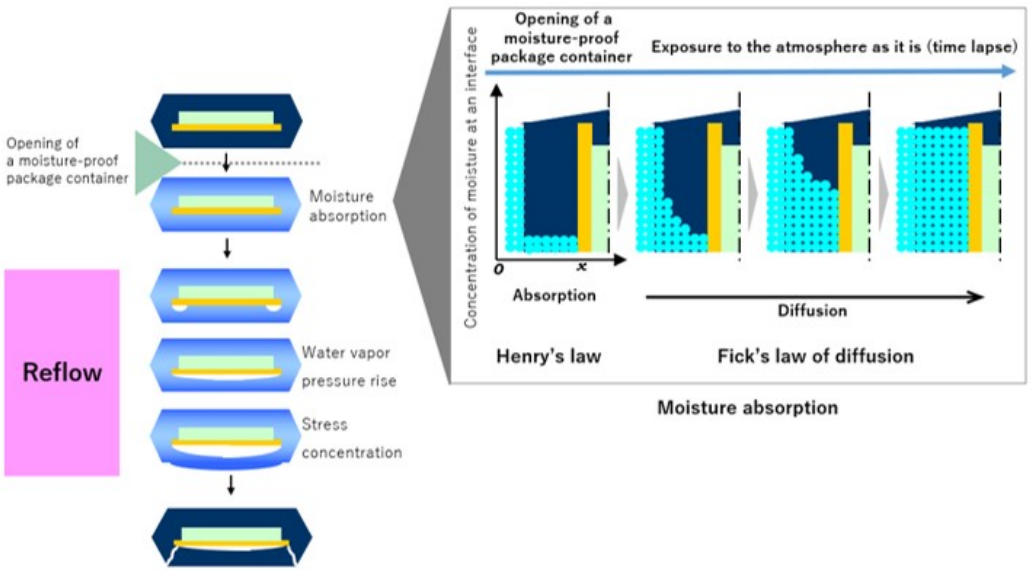


Figure 6-1 Package cracking phenomenon

① When the moisture-proof package container is opened and an SMD is exposed to the atmosphere of storage or a mounting process, atmospheric moisture is absorbed into the surface of the resin forming the package and diffuses to the inside of the package. This diffusion progresses over time, and the moisture reaches the interface between the chip or die pad and the resin inside the package.

② When soldering is performed by reflow or another method that heats the entire package in the condition of ① above, the entire SMD is exposed to high temperature, and this causes moisture at the interface to vaporize and expand. As a result, the water vapor pressure inside minute gaps at the interface rises abruptly, and then this causes stress to concentrate at the edges of the chip or die pad. When this stress exceeds the strength of the resin to be applied when heated, a package cracks.

③ A failure caused due to cracking of a package varies depending on which part of the package cracks.

When a chip side cracks, a wire that electrically connects the chip and the leads may be disconnected, or the interface between the resin and the chip may be delaminated, and then these failures may cause the humidity resistance to deteriorate. When the die pad side cracks, the package expands when solder melts, which may result in a soldering defect.

(2) Factors causing a package to crack: Concentration of moisture at an interface

As described above, moisture absorption of a package is an important factor causing a package to crack. However, more strictly speaking, the factor is not the absolute total of the absorbed moisture, but the concentration of moisture at the interface between the chip or die pad and the resin inside the package.

The moisture absorption process and derivation of the concentration of moisture at the interface are described below. (See Figure 6-1.)

Generally, when solid materials are exposed to the atmosphere, water molecules are adsorbed into the surface mainly by the van der Waals interaction. The organic materials used in SMD packages are said to have stronger affinity to water molecules with compared to inorganic materials.

The concentration of moisture adsorbed into the package surface Qs is expressed by the following expression in accordance with Henry's Law, where S is a solubility coefficient unique to a material and Pa is the atmospheric water vapor pressure.

$$Qs = S\,Pa \qquad \cdots\cdot \text{Expression 6.1.1}$$

Here, the solubility coefficient S can be expressed by the following expression, where Es is the activation energy and T is the temperature.

$$S = So \exp(Es/kT) \qquad \cdots\cdot \text{Expression 6.1.2}$$

k: Boltzmann constant So: Constant

The moisture adsorbed into the package moves to the inside of the package until the diffusion phenomenon is eliminated, that is to say, until the concentration gradient is eliminated. At this time, moisture on the package surface is constantly supplied from the atmosphere, and the concentration of moisture determined by Expression 6.1.1 is maintained. The diffusion phenomenon follows Fick's law of diffusion within the environmental temperature range of the SMD storage and mounting processes, and can be expressed by the following expression,

where *D* is the diffusion coefficient, *x* is a position coordinate and *t* is time.

$$\frac{\partial Q(x,t)}{\partial t} = D\frac{\partial^2 Q(x,t)}{\partial x^2} \quad \cdots\cdot \text{Expression 6.1.3}$$

The diffusion coefficient D is expressed in the following expression, where Ed is the activation energy and T is the temperature.

$$D = Do \exp(Ed/kT) \quad \cdots\cdot \text{Expression 6.1.4}$$

k: Boltzmann constant Do: Constant

From the above equations 6.1.1 to 6.1.4, it is possible to obtain interfacial moisture concentration which is a factor causing package cracking. At the Semiconductor Business Unit, we evaluate the resistance to package cracks focusing on this interfacial moisture concentration to determine the implementation level for each product.

(3) Factors causing a package to crack: Package exposure temperature during soldering

As described above, a package cracks when moisture that has reached an interface evaporates and expands abruptly during soldering, and then the internal stress exceeds the thermal strength of the resin that composes the package. As the temperature to which the package is exposed gets higher, the probability of cracking increases. This is caused due to the water vapor pressure generated inside the gaps of the package interface and the temperature dependence of the strength of the resin composing the package.

For example, when comparing exposure temperatures 220 °C and 260 °C, the temperature dependence of the saturation water vapor pressure shows that at 260 °C, the water vapor pressure rises approximately twice and the resin strength is lowered to approximately a half. (See Figures 6-2 and 6-3.)

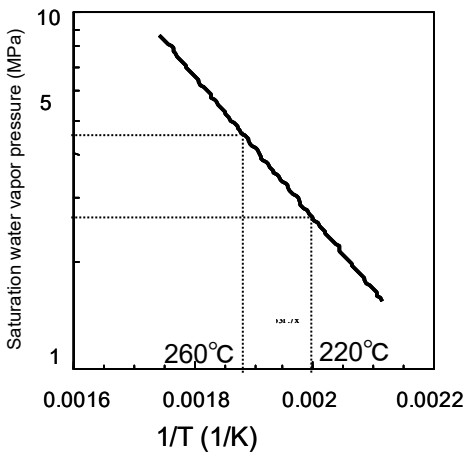


Figure 6-2 Temperature dependence of the saturation water vapor

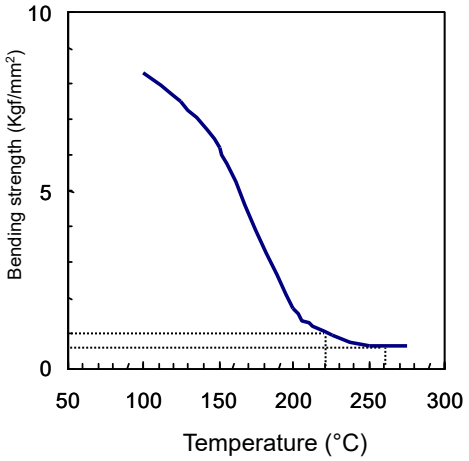


Figure 6-3 Temperature dependence of the mold resin bending strength

(4) Factors causing a package to crack: Package structure and materials

Even though an SMD is exposed to the same ambient conditions for the same period of time before soldering, the concentration of moisture on an interface, which is a factor causing a package to crack, shows a different value according to the thickness, solubility coefficient and diffusion coefficient of the resin over a semiconductor chip or under a die pad that functions as the diffusion path.

In addition, the stress σ generated inside the solder is expressed by the following expression based on a uniform load model whose circumference is fixed, where a is the shorter side of the chip or die pad, k is a coefficient determined by the ratio between the shorter side a and the longer side b, h is the thickness of the resin over the chip or under the die pad, and P is the water vapor pressure inside the package. (See Figure 6-4.)

$$\sigma = 6k(a/h)2P \quad \cdots\cdots \text{Expression 6.1.5}$$

Therefore, even though the concentration of moisture on the interface or the exposure temperature during soldering, which is another factor causing a package to crack, are the same, the cracking occurrence rate becomes different when the semiconductor chip or die pad size is different.

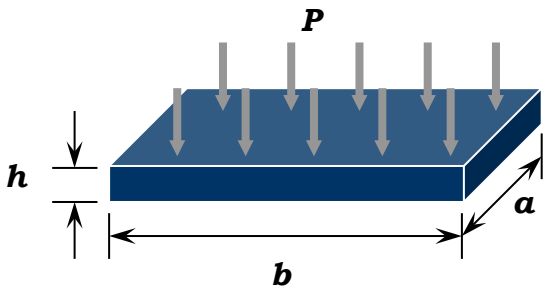


Figure 6-4 Uniform load distribution model whose circumference is fixed

6.1.2 Notes on Cracking of a Package

(1) When mounting a product on your device, you have to satisfy the following requirements: allowable time and allowable number of times soldering is performed after opening a product package regulated according to the MSL corresponding to the product, and the SMD exposure atmosphere after opening the product package and soldering temperature conditions that are prerequisites for the MSL.

(2) When the lapse of time exceeds the allowable time after opening the moisture-proof package case, products can be used by baking to remove moisture. However, the baking conditions that reduce the concentration of moisture on the interface to an appropriate value vary depending on packages. Contact our sales representative when baking is necessary.

(3) When the moisture-proof package case is opened but products are not mounted on any of your devices yet, store them under the following conditions: 30°C and 30%RH or less.

(4) Moisture enters the inside of the moisture-proof package case even through the package case is scratched even a little. As a result, packages inside the case may crack even under the conditions recommended by the MSL. Be sure to take care to handle the package case of SMD packages.

(5) Minute amounts of moisture permeate the laminate bags of even unopened moisture-proof package case. Avoid storing packages for a long time.

<Reference materials>

1) Kansai Electronic Industry Development Center, Reliability Subcommittee, “Survey Report of Documents Concerning the Pressure Cooker Test” (1983)

2) Nanjo, “Materials and Moisture Handbook,” Society of Polymer Science, Polymer and Moisture Absorption Committee (1968)

3) Saito and Hirai: Practices in Mechanics of Materials

6.2 Notes on Handling the Electric Breakdown

As the transistor size is getting smaller due to thinning of a gate oxide film and miniaturization of wiring, the resistance of a semiconductor device to electric stresses such as electrostatic discharge (ESD), overvoltage and overcurrent (electric over stress: EOS) is lowered, and this is a serious problem. Even slight voltage fluctuations and noise penetration that were not a problem thus far are becoming increasingly likely to cause a device to malfunction or break down.

This section describes countermeasures for preventing semiconductor devices from malfunctioning or breaking down due to electrical stress.

6.2.1 Electrostatic (ESD) Breakdown

6.2.1.1 Charging Phenomenon of Static Electricity

Charging of static electricity means that when electric charges that are moved as a result of contact of two objects remain on the objects even after the objects are separated, and then the objects holds the electric charges. When the number of electrons in an object is excessive, it is negatively charged, and when the number of electrons in the object is insufficient, it is positively charged.

Generally, as the electrical properties of objects, they can be classified into two: objects that easily acquire electrons and those that easily give electrons. Table 6-1 shows the Faraday triboelectric series. When a higher item of the triboelectric series comes in contact with or rubs against a lower one, the higher item gives electrons to the lower one and becomes positively charged, while the lower item acquires electrons from the higher one and becomes negatively charged. Table 6-2 shows an example of typical electrostatic charging voltages.

Table 6-1 Triboelectrification series table [1)]

Positive (+)	Acetate
	Glass
	Nylon
	Wool
	Silk
	Aluminum
	Polyester
	Paper
	Cotton
	Steel
	Nickel, copper, silver
	Zinc
	Rubber
	Acrylic
	Polyurethane foam
Negative (-)	PVC (vinyl)
	Teflon

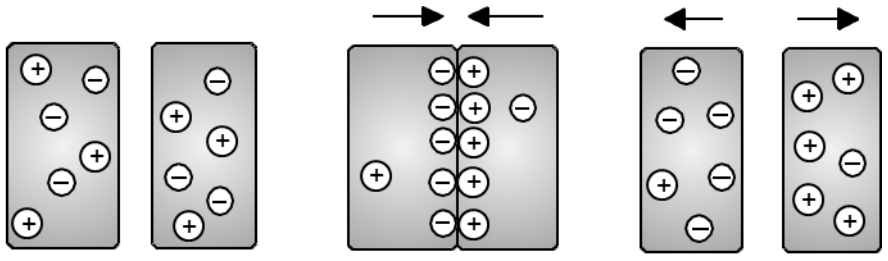
Table 6-2 Typical electrostatic charging voltage

Static electricity generation sources	Charging voltage	
	Relative humidity 10 % to 20 %	Relative humidity 65 % to 90 %
Walking on a carpet	35,000 V	1,500 V
Walking on plastic tiles	12,000V	250 V
Person working at a general workbench	6,000 V	100 V
Card case	7,000 V	600 V
Plastic bag taken from a workbench	20,000 V	1,200 V
Urethane foam cushion chair	18,000 V	1,500 V

Two main mechanisms for generating static electricity that causes the electrostatic discharge phenomenon in the processes where semiconductor devices are handled are as follows.

(1) Charging due to contact and separation (friction) between objects

When two objects touch each other, charges migrate between the objects on the contacting surfaces (Figure 6-5 (a) – (b)). When the objects are separated in this condition, charges remain on the surface of each object in the deviated state, and becomes electrostatically charged (Figure 6-5 (c)). Generally, triboelectric charging is supposed to cause static electricity to be generated, and can be regarded as the following condition: contact and separation occur repeatedly in this manner.



(a) Normal condition **(b) Charges migrated due to contact between two objects** **(c) Separation of objects (charged)**

Figure 6-5 Mechanism of charging caused due to contact and separation of objects

(2) Charging induced from charged objects

When a charged object comes close to an insulated conductor, the inside of the conductor is affected by an electrical filed from the charged object, and then electrostatic induction causes a deviation in charges. In this condition, the conductor is causing induction charge (Figure 6-6 (a)). If a part of the conductor is grounded (GND) or made to contact with another conductor when induction charge is caused and electric charges get nonuniform, a charge having the same polarity as that of the charged object that has moved close to the conductor moves from the conductor to the GND or another conductor, and an electrostatic discharge phenomenon occurs (Figure 6-6 (b)). Furthermore, if the conductor is separated from the GND and the charged object is moved away from the conductor, the charges in the conductor that were attracted to the charged object become free and there are too many charges inside the conductor, and then they are electrified to have the same polarity (Figure 6-6 (c)). If a part of the conductor is made to contact with the ground or another conductor again in this condition, the electric charges are discharged (Figure 6-6 (d))

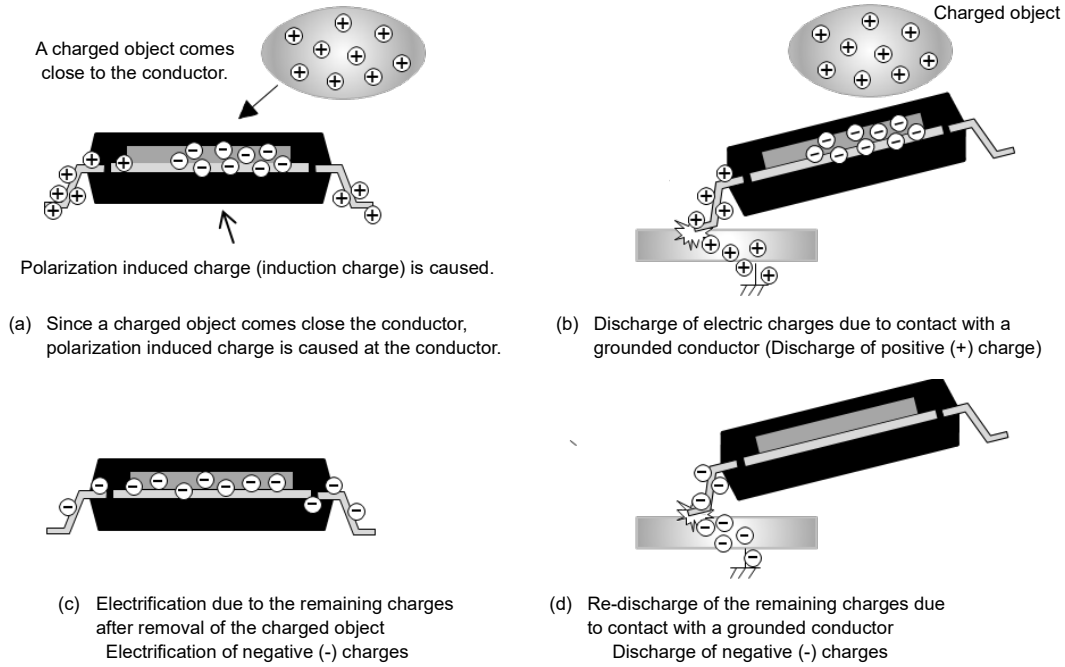


Figure 6-6 Inductive charges caused by approach of a charged object and the second discharge phenomenon

If this charging phenomenon is applied to a semiconductor device, a chip and a lead frame section are equivalent with this conductor. Just by bringing a charged object close to an insulated semiconductor device, a chip is inductively charged. When you bring its terminal into contact with metal, it may discharge static electricity. In addition, the surface of a plastic package is charged due to friction or any other reason, it plays a role of a charged object, which causes a chip to be charged inductively, and this leads to discharge of static electricity due to inductive charging in the same manner.

Such an inductive charging is caused not only at a semiconductor device but also at ungrounded metal, tweezers and tools you hold by wearing insulative gloves or finger stall, a wiring pattern of a PCB board and metal wiring of a flexible board. These items may cause the discharge of static electricity at a semiconductor device in a mounting process.

In this way, removal of a charged object that causes induction charge in a process for handling a semiconductor device is an important countermeasure also.

6.2.1.2 Electrostatic Discharge Destruction Test Method

Electrostatic discharge phenomena occurring when semiconductor devices are handled are classified into several models according to charged objects and the discharge styles. The test methods used to evaluate the electrostatic discharge resistance of a semiconductor device are devised based on these electrostatic discharge modes.

(1) Human Body Model (HBM) [3), 4), 5)]

The human body model (HBM) is a model for discharging static electricity accumulated in a charged human body to a semiconductor device. This is a testing method that uses the capacitance of the human body (= 100 pF) and the contact resistance between the human body and the device (= 1500 Ω) for a discharging circuit. Since this testing method has been used for a long time in the U.S. MIL standard (MIL-STD-883D method3015.7), and is thus widely used as a standard ESD test method of a semiconductor device in Japan and overseas.

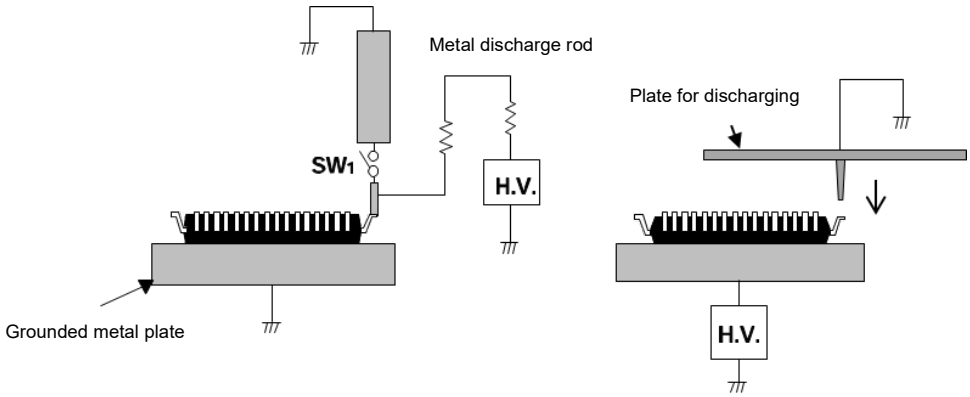
(2) Machine Model (MM) [3), 6)]

The machine model ESD testing method was originally devised as one of human body discharge models based on the human body capacitance and the worst discharge resistance (200 pF/0 Ω). This testing method has been used by semiconductor device manufacturers in Japan mainly as a means for discovering circuits that are not resistant to electrostatic breakdown to verify the device design. However, it is found that human body discharge phenomenon can be verified by using the human body model (HBM), and that the machine model (MM) simulates excessive discharge phenomena that almost never occur in an actual process due to excessive inductance component (≒ 750 nH) of the discharge path. The MM has been, therefore, deleted from the semiconductor test standards.

(3) Charged Device Model (CDM) [7) to 11)]

The charged device model (CDM) is a testing method that models the following phenomena: static electricity is charged on a semiconductor device itself or charges inducted to the device from a charged object located near the device are discharged. As the characteristics of this model, it reproduces the discharge mechanism in the form closest to the discharge phenomenon occurring in the real environment, so correlations with the ESD destruction modes occurring in processes have also been widely confirmed.

The charged device model testing methods are shown in Figure 6-7. As the charged device model, there are two testing methods: one connects a high voltage source to the device side and accumulates electric charges in the parasitic capacitance between a grounded electrode plate and the device, and then discharges the accumulated charges to the GND via a metal discharge rod by closing SW1 that is connected to a device terminal. This is a contact type discharge method (Figure 6-7 (a)). The other one applies high voltage to a metal plate holding the device to cause induction charge, and then brings the grounded metal plate (plate for discharging) into contact with the terminal of the device to discharge. This is an aerial discharge method (Figure 6-7 (b)). The charged device model repeats charging and discharging each terminal of the device to be tested, and then evaluates the resistance of the device by finally applying stress to all terminals.



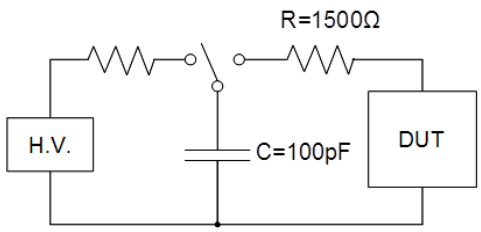
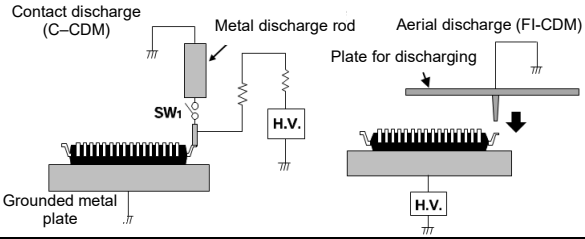
(a) Contact type discharge (C - CDM) **(b) Aerial discharge (FI - CDM)**

Figure 6-7 CDM/FICDM test methods

(4) ESD test standards

ESD testing methods adopted by the current standards are shown in Table 6-3. Respective testing models of the HBM and CDM models are used as standards, and as for the human body model (HBM) tests, almost common tests are performed in Japan and overseas. In the Japanese JEITA standard, the charged device model (CDM) uses a test method that brings a discharge electrode into direct contact with a terminal of the device to inject/discharge electric charges to/from the terminal. In the U.S. JEDEC standard, the Field Induce CDM (FIDM) test method is used to electrify the device with induction charge from the electrode plate to which high voltage is applied, and then brings a discharge electrode into contact with it to discharge the electricity.

Table 6-3 ESD testing methods of a semiconductor device

ESD model	Test circuit	Test standard
Human body model (HBM)	C=100 pF, R-1500 Ω Single discharge 	JEITA EIAJ ES-4701/304 (2013) ANSI/ESDA/JEDEC JS-001-2017
Charged device model (CDM)		JEITA EIAJ ED-4701/305C (2013) ANSI/ESDA/JEDEC JS-002-2014

C-CDM: Contact CDM
FI-CDM: Field Induced CDM

6.2.1.3 Failure Mechanisms due to Electrostatic Discharge Destruction

The main ESD destruction mechanisms of semiconductor devices include the following two phenomena.

(1) Thermal destruction (joint breakage, fusing in wiring)

(2) Insulation film breakdown (gate oxide film breakdown, inter metal dielectric breakdown)

(1) Thermal destruction

Thermal destruction phenomena mainly include PN junctional disruption and melting of metal wiring. Although PN junctional disruption occurs due to relatively low energy such as electrostatic discharge, melting of wiring generally requires high energy, so it is supposed to occur as a result of not electrostatic discharge but electric over stress (EOS) phenomena such as surge and soldering iron leak currents.

A PN junctional disruption phenomenon occurs since excessive current flowing through the junction causes the temperature to rise locally in the junction and exceed the melting point of silicon (1415 °C). In the process, they may be caused by discharge from a charged worker (human body) or discharge of electric charges accumulated in a mounted component and board whose capacity is large such as a mounted board and a capacitor in some cases. In the ESD destruction test, these phenomena can be observed as the destruction mode of the human body model (HBM).

(2) Insulation film breakdown

Insulation film breakdown is a failure mechanism for short-circuiting a gate oxide film or an inter metal dielectric. Insulation film breakdown occurs frequently at devices equipped with a thin gate oxide film among MOS transistors, and this is an ESD destruction failure mechanism seen in the process most frequently. Since the energy required for destruction is small, this phenomenon is caused by the smaller quantity of charges than the thermal destruction, and it is the main ESD destruction phenomenon caused in a process. This insulation film breakdown is known as the main destruction mechanism of the charged device model (CDM), and can be reproduced by a CDM test.

6.2.2 Electrostatic Countermeasure

The gate oxide film thickness of MOS transistors manufactured by the leading-edge processes has already been reduced to several nm or less, and the withstand voltage of these oxide films is only several voltage. As a countermeasure for static electricity, semiconductor devices are equipped with a protection circuit for each input/output terminal against external static electricity so that static electricity cannot be applied to any of internal transistors. However, it becomes extremely difficult to protect the internal transistors against external static electricity exceeding several 100 V by using this protection element.

Furthermore, as the operating frequency of the device increases, the effect of the parasitic impedance of a protection element on the operating speed cannot be ignored, and reduction of the size of a protection circuit is required or the number of terminals that cannot be equipped with this protection circuit increases. As a device is miniaturized or its operation speed is accelerated, the resistance to static electricity of the device is lowered.

Against this background, a countermeasure against ESD destruction becomes increasingly important in processes for handling semiconductor devices. General knowledge required to protect semiconductor devices from electrostatic destruction when handling them, methods for controlling static electricity in processes, and countermeasures against electrostatic destruction are described below.

6.2.2.1 Basic Concept of a Countermeasure against Static Electricity

The basic concept of a countermeasure against static electricity in a process for handling a semiconductor device is described below.

(1) Designing processes and facilities that do not generate static electricity

During process design or in a stage for determining installation of manufacturing facilities, you can establish the manufacturing process including the effective countermeasure for static electricity by installing electrostatic countermeasure facilities (such as grounding, floors and environment.) and incorporating countermeasures for preventing static electricity from being generated due to friction or contact into the equipment specifications.

(2) Not bringing items that are easily charged by static electricity into processes

Electrostatic destruction caused due to friction or induction charging can be prevented by not bringing insulated substances and packing materials such as paper, fixtures and office supplies that easily generate static electricity into processes except when absolutely necessary.

(3) Quickly relieving static electricity to prevent electrostatic discharge

The opportunities for static electricity to discharge to semiconductor devices can be reduced when you quickly release generated static electricity by using various methods such as grounding of equipment and jigs, controlling of resistance values of floors and workbench surfaces, and neutralizing electrostatic charges with an ionizer. In addition, static electricity can be gradually released without causing electrostatic destruction due to sudden discharge when a metal portion to be brought into contact with a device is replaced with a material whose resistance value is appropriate.

(4) Periodically checking the condition of the countermeasures for static electricity and maintaining effects of the countermeasures

After implementing countermeasures against static electricity, the effects of these countermeasures cannot be maintained unless you check the effects periodically, and control them to ensure that they are reliably maintained.

(5) Making workers and managers in charge of process conscious of necessity of countermeasures against static electricity

To implement countermeasures against static electricity, workers and/or managers in charge of processes require knowledge and understanding of static electricity. Antistatic items can be even more effective at preventing electrostatic destruction depending on the awareness of the person using them. Electrostatic discharge problems cannot be solved simply by installing antistatic items. Ensuring thorough implementation of these countermeasures and instilling of antistatic countermeasure concept can make managers in charge of processes and workers aware of the risk of electrostatic destruction, and this is effective means for reducing electrostatic destruction problems in the processes.

6.2.2.2 Concept of the Process Management Standards

In order to control the amount of electrostatic charge in a process, you have to determine the amount of charge to be used as the management criteria. This management criteria are supposed to be set based on the electrostatic resistance of devices handled in the process. However, which testing method should be used to obtain a static resistance value as the process control reference guideline among the electrostatic destruction testing models for devices described in Section 6.2.1.2 is the most important in determining the management criteria. Even though control criteria are set based on ESD phenomena that do not occur in the process, actual electrostatic destruction cannot be effectively prevented.

Figure 6-8 shows the relation between charged objects existing in a process and electrostatic capacitance (capacitance to the ground). Objects causing ESD in a process generally have different electrostatic capacitances respectively. For example, the electrostatic capacitance of the human body is usually said to be approximately 80 to 200 pF [13) - 16)], which is equivalent to the capacitance used by the human body model (HBM). In contrast to this, most items other than workers that may cause ESD with devices such as tweezers and device pick-up jigs on chip mounters and metal parts of positioning stages have electrostatic capacitance of just fF to 10 pF and more. [16)] In addition, the electrostatic capacitance of semiconductor devices themselves is also mostly within the range of several pF to several 10 pF (Table 6-4). When the electrostatic capacitance of charged objects becomes smaller in this manner, the accumulated electrostatic energy becomes lower even when charged to the same voltage, so semiconductor devices are less likely to experience electrostatic destruction.

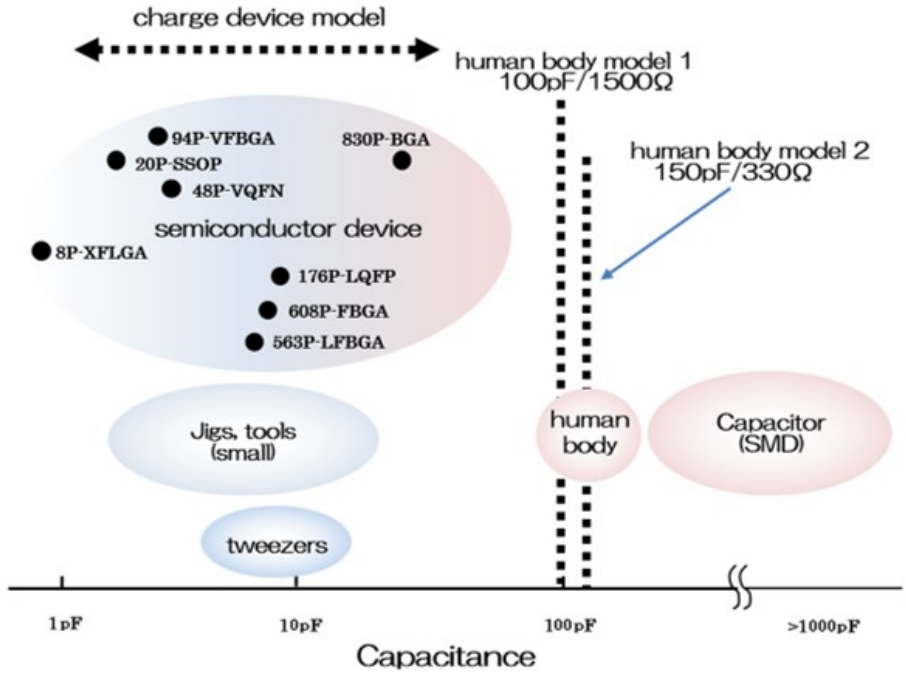


Figure 6-8 Relation between charged objects and testing methods in a process viewed from electrostatic capacitance

Table 6-4 Electrostatic capacitance measurement results of a device package (On a ground plate when a CDM test is carried out)

Package	Electrostatic capacitance (pF)	Package	Electrostatic capacitance (pF)
SSOP-20pin	2.0	BGA-830pin	16.4
LQFP-176pin	9.3	FBGA-608pin	8.5
VQFN-48pin	4.4	VFBGA-94pin	3.8
XFLGA-8pin	0.6	LFBGA-563pin	7.9

In most cases, destruction caused by a discharge phenomenon of static electricity accumulated in small electrostatic capacitance is clearly different from failure modes to be applied when static electricity is discharged from the comparatively large capacitances (100 pF) such as an HBM test.[17) - 20)] As seen in Figure 6-8, the charged device model (CDM) testing method that uses the parasitic capacitance of the device is the most appropriate testing method for reproducing an electrostatic discharge phenomenon caused by a small capacitance charged object existing in a process.[18), 20) - 22)]

In this manner, it is supposed to be desirable to set an appropriate value as a value for controlling the charge amount of a charged object in a process according to the charged object type. Thus, the more realistic charge amount control criteria can be set by referring to ESD resistance data from the human body model (HBM) for workers (human bodies), and that from the charged device model (CDM) for devices and jigs.

6.2.2.3 Basic Countermeasures against Electrostatic Discharge [23), 24)]

In a process for handling a semiconductor device sensitive to static electricity, an ESD protected Area (EPA) should be specified to implement the countermeasures against static electricity described below.

(1) Countermeasures for the human body

Workers who directly handle semiconductor devices or boards on which devices have been mounted should wear both wrist straps and ESD protective shoes. Be sure to use a wrist strap equipped with a cable. If a worker uses a wrist strap without connecting his/her body and the ground with the cable constantly, the charge potential of the human body cannot be held to a low level. Note that the cable may be broken if a sudden load is applied to the cable while the worker is operating.

Be sure to use a wristband in close contact with the bare skin. If the wristband is worn over clothing, the necessary resistance value between the human body and the ground cannot be secured.

If any sole of ESD protective shoes is stained, the contact resistance between the human body and the floor increases and the prescribed leakage resistance may not be obtained. In addition, if a worker sitting on a chair places both feet on a footrest or any other pedestal, conductivity between the floor and the human body is not obtained and the constantly required electrostatic leakage effects cannot necessarily be maintained, for example, electrical continuity cannot be obtained between the floor and the human body. Therefore, safety can be most effectively assured by having workers who directly handle devices wear both wrist straps and ESD protective shoes.

ESD protective gloves and fingerstalls should be used. In particular, the fingerstalls used when handling a device or a board with bare hands must be conductive or have electrostatic diffusion. If the surface of fingerstalls becomes charged, an electrostatic charge is induced in a device when the device is held, and then a discharge phenomenon of the charged device model (CDM) is highly likely to occur. (Figures 6-9 and 6-10)

The charged potential of a human body greatly varies depending on a worker’s action. For example, when a worker gets up from a chair, the charged potential may rise abruptly in some cases. (Figure 6-11)

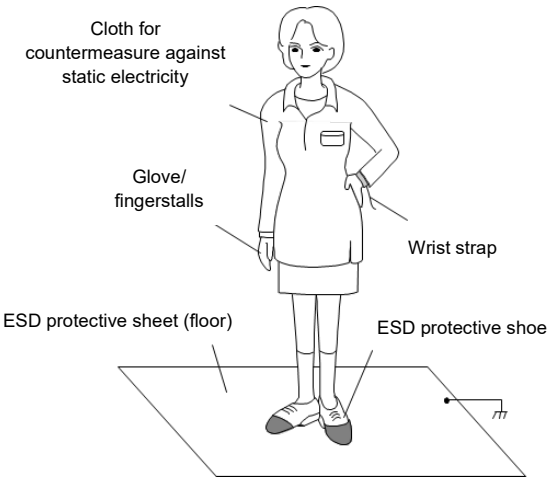


Figure 6-9 Countermeasure example of a human body (worker)

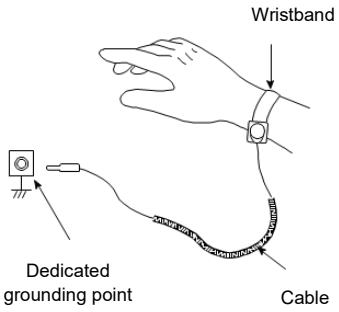


Figure 6-10 Wrist strap usage example

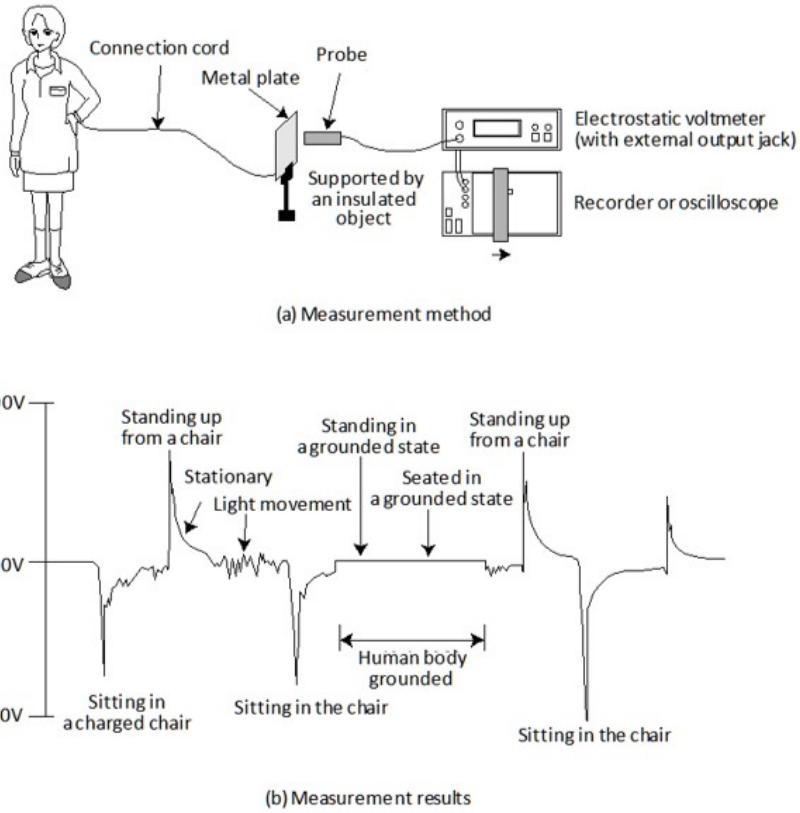


Figure 6-11 Change in the charged potential of a human body

(2) Workbench

The surface of a workbench should be covered with ESD protective sheets (made of conductive materials or materials having electrostatic diffusion) or a workbench should be made of materials having the same characteristics, and it should be grounded. (Figure 6-12). Any insulated object that is likely to generate static electricity should not be placed on the workbench. Fixtures and jigs required for work should be made of conductive materials or materials having electrostatic diffusion, and when it is absolutely necessary, an ionizer should be used. The use of insulated objects that may be in contact with or moved close to devices should be avoided whenever possible especially during work. Avoid placing insulated sheets or plates on a workbench to work.

(3) Chairs

The surface of a part of a chair on which a worker sits on and the backrest of the chair should be protected with an ESD protective cover, or an ESD protective chair should be used. (Figure 6-13) The grounding path from the chair to the floor should be secured with casters having electric conductivity. Static electricity with an extremely high potential may be generated momentarily due to peeling charge between the cloth and the seat surface or the backrest when you get up from the chair. (Figure 6-11)

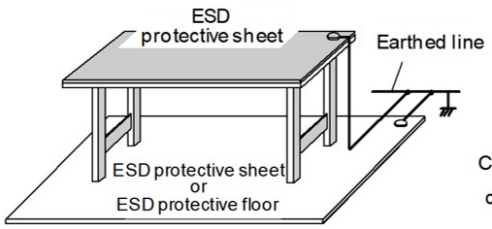


Figure 6-12 Countermeasure example of a workbench

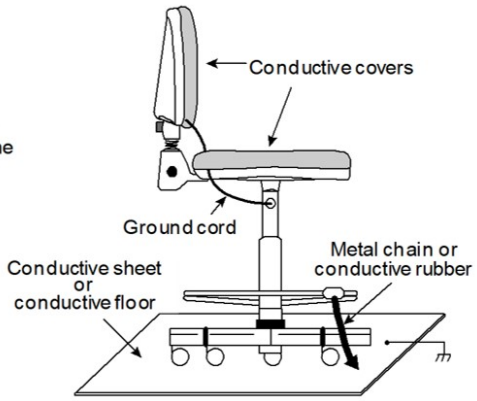


Figure 6-13 Countermeasure example of a work chair

(4) Floor

Floors in the work area should be ESD protective floors or covered with ESD protective sheets. When the entire work area floor cannot be covered with the protective sheet, ESD protective sheets should be laid over at least the work area where workers wearing ESD protective shoes handle devices or boards on which devices have been mounted. When laying ESD protective sheets, be sure to connect all of the sheets to the ground. (Figure 6-12)

(5) Equipment and facilities

Be sure to connect the main units of equipment such as mounters and measuring instruments, and those of facilities for transportation to the ground. Metal parts that are isolated from the grounded main unit by insulators and may come in contact with a device should be grounded individually. Insulator parts that may come into contact with or be moved closed to a device should be changed to materials having electrostatic diffusion characteristics or electricity

charged on them should be eliminated using an ionizer.

Use tools such as electric screwdrivers and soldering irons equipped with a ground type power supply cable for connecting their respective main units or tips to the ground. Or, Electric Over Stress (EOS) destruction may be caused by AC voltage leakage.

(6) Environment

It is generally said that as the humidity (concentration of moisture in the air) is higher, static electricity cannot be generated easily. However, it is not to say that any static electricity is not generated, but the ratio of the leaked charge to the generated charge increases due to moisture adhered to the surface, so that static electricity appears not to be charged easily as a result.

For humidity control of a process, it is important to maintain a humidity environment that makes it difficult for static electricity to be generated. In an actual process, however, heat generated by equipment and other factors in a process creates many spaces whose temperature is high (that is, low relative humidity). Furthermore, all of boards that generate heat when the power is on, components packed in plastic trays or bags, and products stored in a dry warehouse for a long time are not necessarily in a condition that does not allow static electricity to be generated easily. Therefore, it is extremely dangerous to think that since static electricity cannot be generated easily by increasing the humidity, other electrostatic countermeasures can be simplified. Humidity environment management must be regarded only as an auxiliary electrostatic countermeasure.

(7) Storage and transportation

Semiconductor devices should be stored in the packaging form for shipment. Correctly storing devices in the same ESD protective packing materials as when shipped reduces the risk of electrostatic destruction even when devices are handled during storage.

In addition, boards on which devices are mounted must be stored in containers or on storage shelves made of a conductive material or a material having electrostatic diffusion (Figures 6-14 and 6-15). At this time, use of insulated partitions or storage in insulated bags should be avoided. Since mounting boards themselves are made of insulating materials, the boards may be charged due to vibration or rubbing during storage or transportation. Furthermore, if they are placed near a charged object, an induction charge may be generated on the wiring pattern of the board, and it may be discharged from the connectors during measurement or assembly, and then destroy the device.

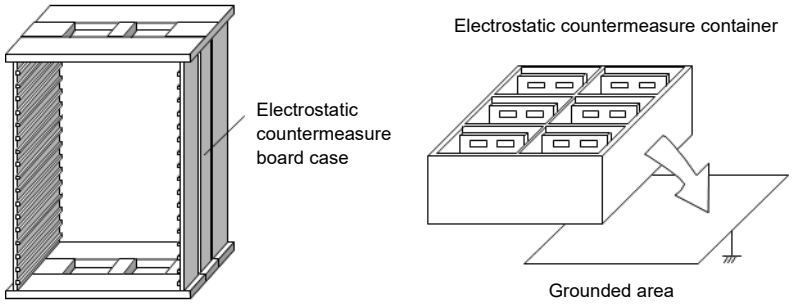


Figure 6-14 Electrostatic countermeasure example of a case for storing boards

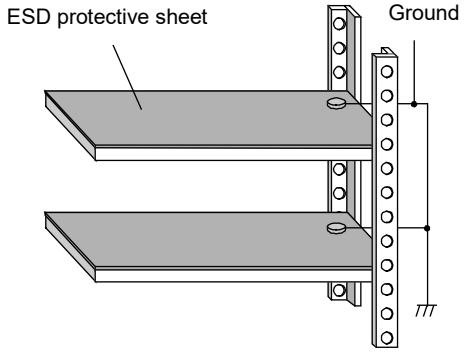


Figure 6-15 Electrostatic countermeasure example of storage shelves

(8) Mounted/assembled components other than devices

Many board mounted components other than semiconductor devices are electrostatically charged while components are mounted on a board or board mounted components are stored. Board mounted components such as capacitors, filters, LCD boards for display and flexible connectors that consist of metal and insulating material and have capacitances capable of accumulating static electricity may cause ESD when they are mounted on a board, and then destroy devices.

Parts boxes used to store these components and packing for delivery must have electrostatic countermeasures. (Figure 6-16) You have to take countermeasures for recognizing that static electricity is charged on some mounted components other than devices, and then preventing these components from discharging static electricity while they are mounted on a board.

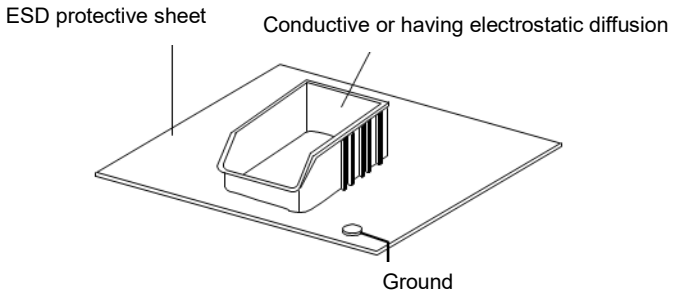


Figure 6-16 Electrostatic countermeasure example of a parts box

(9) Modules and set components

Module components on which a semiconductor device is mounted such as optical pickups and camera modules may cause ESD destruction when a module is handled alone. Even after a semiconductor device is mounted on a module, it should be handled as a single semiconductor device if any terminal is directly exposed to the outside via a connector.

In the set product assembly process, a component consisting of metal and insulating materials such as metal chassis and cables, and an assembled component such as an LCD panel for displaying, an optical disc drive, an optical pickup and various modules may be charged, discharge static electricity to a mounted board via connectors during assembly of the set product, and then destroy a semiconductor device. Fully pay attention to assemble a set product so that it cannot be charged.

(10) Eliminating charges using an ionizer

An ionizer is a neutralization apparatus that generates corona discharge by applying a high voltage to the tip of a discharge electrode needle, and then neutralizes static electricity with the generated ions. This is an effective means for eliminating static electricity from insulating material from which static electricity cannot be released by grounding. Unlike charges on metal, charges on insulating material cannot destroy a device by themselves by being discharged to it. However, these charges may generate induction charges in a device and metal parts, and then cause static electricity to be discharged. When an insulating material is used near a device, it is effective to use an ionizer to neutralize static electricity charged on the surface of the insulating material [25)].

The charge eliminating performance (charge eliminating time) of an ionizer varies greatly depending on its elimination method. Select an ionizer that is designed to eliminate charges appropriately according to an object whose charges are to be eliminated or the use environment. Be sure to measure the ion balance and the charge eliminating capability periodically and perform the appropriate maintenance to maintain its charge eliminating capability.

(11) Clothes

A worker should make efforts to wear clothing made of materials that do not generate static electricity easily. Clothing made of materials that easily generate static electricity (such as chemical fiber) is highly likely to induce strong static electricity in human bodies as the worker acts.

(12) Characteristics required for ESD protective items

Use the values given in Table 6-5 below as a reference for the characteristics required of the main ESD protective items. Even when the characteristics described in the Specifications satisfy the required standards, be sure to fully confirm the effect of the countermeasures actually taken before selecting ESD protective items to be installed.

Table 6-5 Characteristics required of the main ESD protective items [26), 27)]

ESD protective item	Range of resistance value	Remarks
Floor	$Rg < 1 \times 10^9\,\Omega$	
ESD protective sheet (Floor, surface of a workbench, storage rack)	Point-to-point resistance $1 \times 10^4 \leqq Rp \leqq 1 \times 10^{10}\,\Omega$ EPA-to-ground resistance $7.5 \times 10^5 \leqq Rg \leqq 1 \times 10^9\,\Omega$	See Note 1.
ESD protective shoes (When worn on a metal plate)	EPA-to-ground resistance $1 \times 10^5 \leqq Rg \leqq 1 \times 10^8\,\Omega$	
Wrist strap (band)	Resistance value $Rp \leqq 1 \times 10^5\,\Omega$	
Wrist strap (cable)	Resistance value between terminals $7.5 \times 10^5 \leqq Re \leqq 5 \times 10^6\,\Omega$	
Wrist strap (when worn)	EPA-to-ground resistance $7.5 \times 10^5 \leqq Rg \leqq 3.5 \times 10^7\,\Omega$	
Chair	EPA-to-ground resistance $Rg \leqq 1 \times 10^{10}\,\Omega$	
Clothes	Point-to-point resistance $1 \times 10^5 \leqq Rp \leqq 1 \times 10^{11}\,\Omega$	

Note 1: EPA: ESD protected area

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6.2.3 Electromagnetic Compatibility (EMC)

6.2.3.1 What is EMC?

Semiconductor devices and system circuits may malfunction or their functions may deteriorate depending on the electromagnetic environment. This is because noises generated from power supply circuits that use high-speed switching, digital circuits and printed wiring boards inside the equipment are combined with one another, and then emitted via various paths, and they affect semiconductor device and system circuit operation together with the effects from external equipment. Recently mounting density and frequency have increased and analog-digital mixed systems have evolved, and these factors have further complicated this situation. Furthermore, functions are integrated to semiconductor devices or semiconductor devices are modularized, so that semiconductor devices are provided not as individual parts but like conventional set products viewed from their functions. Therefore, they tend to be required of the EMC performance that satisfies the compliance requirements by themselves.

To address these problems, it is important to identify noise sources and understand transmission paths. Appropriate measures such as reinforcement of GND, optimization of circuit layout patterns, and application of electromagnetic shielding and electromagnetic wave absorbers to semiconductor devices and set circuits must be taken to prevent the problems.

EMC is regulated by International Electrotechnical Commission (IEC) and Comité international spécial des perturbations radioélectriques (CISPR) as the international standards, Voluntary Control Council for Interference by information technology equipment (VCCI) in Japan, and the corresponding standards of each country.

6.2.3.2 About EMC/EMI/EMS

Performance that suppresses electrical noises emitted from electronic equipment and prevents electronic equipment from causing troubles such as malfunction due to surrounding electrical noises is referred to as Electromagnetic Compatibility (EMC).

As for EMC, “emission” indicates unnecessary electric noises (mainly electromagnetic waves) emitted from electronic equipment or components such as semiconductor devices. Noises emitted from these devices may affect operation of another electronic equipment or radio equipment via air or via an electrical wire. This is referred to as “Electromagnetic Interference” (EMI). To prevent an electromagnetic interference from occurring, the emission level of all pieces of electronic equipment is required to be within the range regulated by the standards and/or directives.

As for EMC, “immunity” indicates a capability of electronic equipment and parts such as semiconductor devices for enduring against electric stress (such as an electric field, a magnetic field, voltage and current) when they are exposed to the stress. This performance is referred to as “Electromagnetic Susceptibility” also. Electronic equipment is exposed to various types of electric stress depending on their respective use environments. Electric stress is generated from radio wave of wireless communication or public broadcast as well as from electronic equipment or parts such as semiconductor devices. In addition, electric stress generated by natural phenomena such as thunder and static electricity has to be considered also. In the same manner as emission, all pieces of electronic equipment have to have immunity required to prevent any electromagnetic interference.

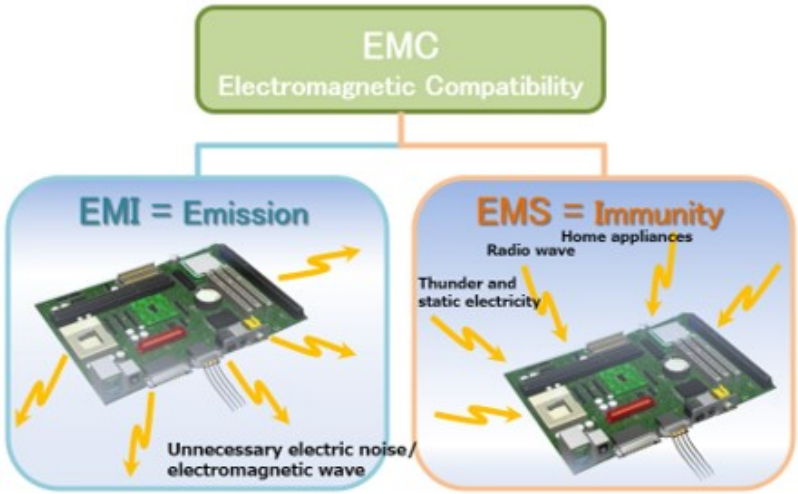


Figure 6-17 Image of EMC/EMI/EMS

6.2.3.3 Standardization Trend of the Semiconductor Device EMC Measurement Methods

6.2.3.3.1 EMI

While the EMI measurement method of electronic equipment is regulated and standardized as compliance items by various standards and directives, any standard measurement methods only for a semiconductor device has not existed until recently. Therefore, a semiconductor device had to be mounted on electronic equipment to be used, and then the entire equipment had to be measured, so that we had no choice but to evaluate the EMI characteristics of the equipment including the semiconductor device. However, there are many problems as follows: ① if there is a noise source other than the semiconductor device to be evaluated, it is difficult to quantify contribution of the desired semiconductor device, ② when two different semiconductor devices are compared with each other, a board of equipment has to be prepared for each semiconductor device, so that the evaluation cost increases. Therefore, this method is not widely used at this point.

As for the EMI evaluation method of a semiconductor device, its international standardization had been reviewed by the IEC as the IEC61967 series, and then the embodied measurement method was standardized as IEC/TS 61967-3-Ed. 2.0 (Surface scan method: Magnetic field probe method) in 2014.

6.2.3.3.2 EMS

The EMS measurement method of electronic equipment is mainly standardized by the IEC 61000 series in case of general electronic equipment, or by the IEC 60601-1-2 in case of medical electronic equipment. However, in the same manner as the EMI, any standard measurement method has not existed for a semiconductor device alone until recently. Although the IEC 61000 series is required in some cases, this is not appropriate as a measurement method of a semiconductor device alone.

Although the IEC 62132 series and IEC 62215 series have been reviewed by the IEC as the EMS evaluation method of a semiconductor device, any international standard is not regulated for it yet.

6.2.3.4 Example of a Semiconductor Device EMC Measurement Method

6.2.3.4.1 IEC/TS 61967-3-Ed. 2.0 Magnetic Field Probe Method: EMI

This is a measurement method that can detect a noise source from a circuit correctly. Although this standard regulates the frequency up to 1 GHz, it can measure the frequency range exceeding 1 GHz depending on the measurement device to be used. For example, we use this method for a semiconductor device used in a GPS product or GPS module receiving a signal whose frequency is 1 GHz or higher to identify the noise source whose bandwidth affects the frequency of the GPS.

6.2.3.4.2 SAE J1752-3 TEM Cell Method: EMI

This measurement method measures the level of noise generated by a semiconductor device by suppressing the effect of the external noise. It is adopted as the AEC-Q100 EMC measurement method, and is required of measurement data as the EMI measurement method for on-vehicle semiconductors. As a measurement device, a square pyramid type TEM cell is used and only a semiconductor device is set inside, so that noise radiated from the semiconductor device can be measured accurately. Noise intensity can be obtained per frequency as measurement data. This method is hardly affected by external noise due to shielding with the TEM cell. However, where noise is generated cannot be identified in the same manner as the magnetic field probe method: this is a disadvantage.

6.2.3.4.3 IEC 61000-4-2 Human Body Model ESD: EMS

This measurement method does not measure the EMS resistance (immunity) of a semiconductor device alone, but it is known to measure the EMS resistance of equipment on which semiconductor device is mounted. This is recognized as the human body model ESD (Electrostatic Discharge) test or the system level ESD test also. This method uses an ESD gun to directly or indirectly discharge to equipment, and then determines whether the equipment passes the test or not according to whether the equipment malfunctions or not. The material and height of a test stand are regulated by the standard. To obtain the highly reproducible test results, the appropriate environment including the test environment has to be established.

6.2.3.5 EMC Required for a Semiconductor

As for EMC, which is a compliance test required for a semiconductor, the IEC 61000 series test is requested to function as an immunity test that checks if the semiconductor does not malfunction due to ESD noise radiated by the system level ESD test when the semiconductor is incorporated into the set product, and the SAEJ1752-3 test of the TEM cell method is requested to function as an emission test for a semiconductor to be used in a vehicle according to the AEC-Q100.

6.2.4 Strong Electric Field and Strong Magnetic Field

Generally, a strong external electromagnetic field hardly destroys a device directly. However, when a device is exposed to a strong magnetic field, an abnormal phenomenon such as change of the impedance and increase in the leak current may occur because a polarization phenomenon occurs inside plastic materials or an IC chip of a package. Special care should be taken in using the devices for which electron spin phenomena etc. are applied.

In addition, if any power supply or a part that generates high voltages is located near a device, large noise via the power supply line or the ground line may cause a circuit to malfunction or the IC to generate noise in some cases.

To prevent these external electromagnetic interferences from causing the circuit to malfunction, a circuit layout pattern and component arrangements on a printed board have to be optimized and shielded wires have to be used. In addition, you have to be careful to design a product, for example, by changing mounting locations or taking electric and/or magnetic field shielding measures as necessary.

6.2.5 Overvoltage Breakdown (EOS Breakdown)

Failure modes in which overvoltage or overcurrent other than static electricity destroys a device are referred to as overvoltage breakdown or electric over stress (EOS) breakdown. Electric over stress has various causes, but many device burnout failures are generally caused by application of pulse-type overvoltage stress that is generally called “surge.” Causes of surge include release of electric charges from capacitive loads due to power-on/off of equipment or relay switching and lightning surge due to lightning.

The mechanism of EOS breakdown caused by surge varies depending on the type of surge to be applied. When voltage exceeding the rating is applied to the power supply or input/output terminals of a device, the following failures occur: a junction breaks downs inside the device or a parasitic transistor is set to ON. If an overcurrent flows and the energy consumed by the metal line or a junction part of a transistor exceeds the line or junction endurance level, the wiring may melt or the junction may suffer thermal breakdown.

As a countermeasure against an EOS breakdown, a voltage clamping diode or capacitor has to be inserted into the power supply or input/output terminals on the board to prevent any surge from intruding into the board. This requires a noise countermeasure such as a measuring instrument used to adjust boards in a process.

6.2.6 Handling a High-frequency Device

As a semiconductor device achieves the higher functionalization and performance, its structure is further miniaturized and made higher in density, oxide films and wiring layers become thinner, and then electrostatic resistance is lowered essentially.

To increase the electrostatic resistance, countermeasures such as insertion of an electrostatic protection circuit into input/output terminals of a device are generally taken, but this also results in degradation of the characteristics on the minus side.

Particularly as for high-frequency and high-speed devices, sufficient electrostatic countermeasures cannot be taken for some terminals in order to satisfy the required performance. For example, although ESD protection elements with high electrostatic resistance and low capacitance are required for input/output terminals of high-speed transmission interface devices such as LVDSs and MIPIs, protection against ESD that allows both the high performance and high resistance cannot be realized easily.

Therefore, a sufficient countermeasure must be taken in all work environments and for handlings from device storage and transportation to mounting on a set product and inspection.

6.2.7 Latch-up

A latch-up phenomenon is as follows: overvoltage or current stress such as static electricity or noise intruding from the outside triggers the parasitic thyristors in a CMOS device and generates a short-circuit between the power supply and GND. Although the latch-up phenomenon occurs in the operating condition (the condition in which a power supply voltage is applied), as long as voltage stress that exceeds the device rating is not applied, a latch-up rarely occurs within the normal operating voltage range. While electronic equipment is being used, a latch-up phenomenon is supposed to occur accidentally mainly because the stress exceeding the rating intrudes into a product into which a semiconductor is incorporated or such a state is generated while the equipment is operating. The followings are supposed to be the causes of a latch-up phenomenon.

(1) Intrusion of static electricity from the outside

If static electricity intrudes into a device that is mounted on a board while it is operating, the discharge current passes through the protective elements of the input/output terminals, and then flows to the power supply or GND wiring. In case of a human body, the peak current value that flows due to several kV ESD can reach several A to several ten A. If this current flows to the power supply or GND wiring of the board, potential fluctuation of the power supply or GND may reach several V and then may exceed the device rating. If this voltage fluctuation occurs while the device is operating, the junctions inside the device may break down and cause a latch-up.

Portable type electronic devices (such as cellular phones, camcorders, notebook computers, portable information terminals and digital cameras) have spread rapidly in recent years, and the chassis of these electronic devices that are frequently and directly touched by people are not grounded. Therefore, these devices are easily affected by fluctuations of the power supply voltage caused by ESD from a human body, and a latch-up phenomenon is highly likely to occur.

(2) Intrusion of lightning surge

Lightning surge intruding via a communication cable or a transmission line is likely to generate a latch-up at a semiconductor device used in communication system facility equipment or power supply facility equipment. Lightning surge intruding through a utility pole, a transmission cable or a telephone line may generate a latch-up at even household electronic products.

(3) Electromagnetic susceptibility (EMS)

If sources of electromagnetic noise (such as a car engine, a cathode ray tube and ESD) are located around electronic equipment, noise induced by a sudden change in the electromagnetic field may generate a latch-up.

(4) Live wire insertion or removal

When a board is inserted to the system while the system is operating to perform maintenance or repair work of a system, voltage is supposed to be applied to the input/output terminals before power is supplied to the board depending on the manner in which the connectors are connected. At this time, the potential of the input/output terminals momentarily become higher than the power supply voltage, and this may cause current to flow from the terminal and then generate a latch-up.

(5) Power supply voltage application sequence of multi-power supply devices

The potential of a certain terminal of a device equipped with multiple different power supplies may rise above the corresponding power supply voltage depending on a sequence in which the power supply voltages are applied, and this may generate a latch-up. You have to pay attention to the order in which voltage of the power supplies are applied to the device equipped with multiple power supplies.

Latch-up generated by external factors in this way can be suppressed by taking countermeasures for preventing surge or noise that serves as the respective triggers from

intruding into a device. As the effective countermeasures against static electricity or a surge that directly intrudes into a terminal, insert an element such as a diode and a capacitor for countermeasures against a surge into the entrance of a board that is an intrusion path, or make the board power supply and GND wiring pattern so that they can be resistant to potential fluctuations and noise. In addition, the following countermeasures are effective also: lower the power supply and GND wiring impedance to suppress potential fluctuations caused due to sudden current, or separate the power supply and GND wiring of a circuit block to which a surge can intrude from the outside easily. As for countermeasures for the power supply application order, insert a capacitor or take another measure to delay the respective rising timings.

As for electromagnetic noise, you have to take the shielding countermeasure to prevent electromagnetic waves from intruding into electronic equipment, and then form wiring patterns that are resistant to induction of an electromagnetic field. When a source of electromagnetic noise is located inside the equipment, you have to take a countermeasure against the noise source or separate the power supply and GND wiring.

6.2.8 Thermal Runaway

Thermal runaway is the following phenomenon: a positive feedback that increases the power corresponding to the temperature characteristics of the IC internal circuit causes the temperature to rise without limit, and then destroys a device. Most of breakdowns occurring after mounting the device are supposed to be caused by thermal runaway. In addition to thermal runaway caused by local heat generation in a device, thermal runaway may also occur depending on the heat radiation structure in case of a power device. Therefore, take special care to design heat radiation.

6.3 Notes on Handling a Device in Case of Mechanical Breakdown

A device should be handled carefully. If a device is dropped or any impact is applied to a device, it may be damaged. Be careful to handle it so that any mechanical vibrations and shocks cannot be given to it as much as possible.

A device is composed of parts such as chips, bonding wires, external terminals, heat radiating fins and mold resin, and the mechanical strength and coefficient of thermal expansion of each composing material are different from one another. Therefore, a mechanical breakdown may be caused in various cases such as forming or cutting of an external terminal, mounting of a semiconductor device onto a printed board, washing, and attaching of a heat radiation plate.

These mechanical external forces may cause a package or chip to crack, and lead to degradation of the humidity resistance due to delamination at the interface between the mold resin and the external terminal.

6.3.1 Forming/cutting of an External Lead

To form or cut an external terminal to be used when mounting a semiconductor device onto a printed board, be careful not to apply unreasonable force to the external lead. (Figure 6-18)

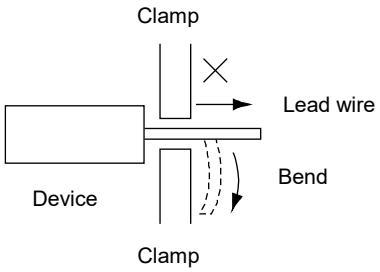


Figure 6-18 Notes on forming/cutting of an external lead

(1) When bending an external lead, fix the external leads between the point at which the lead is to be bent and the package main body. Do not bend any external leads while holding the package main body.
When using a metal mold, do not apply any stress to the package main body either.
When cutting an external lead, do not apply stress to the package main body in the same manner.

(2) Do not repeat bending any external lead.

(3) Do not bend any external lead in the direction of its thickness.

(4) An external lead plating may be damaged depending on how you bend the lead. Be careful to bend the lead.

6.3.2 Mounting a Semiconductor Device on a Printed Board

When mounting a semiconductor device on a printed board, you have to be careful not to apply any unreasonable stress to an external lead. If any external lead is bent or floats from the board, good solder connection state with the printed board may not be obtained, and this may cause a mounting failure. (Figure 6-19)

(1) External leads have to be attached on a printed board with the same interval as that of external leads of a device.

(2) When inserting a device into a printed board, do not insert it forcibly.

(3) Provide an appropriate clearance between a semiconductor device and a printed board.

(4) If any external lead is deformed or floats when a surface mounted-type device is mounted on a printed board, good solder connection state with the printed board may not be obtained, and this may cause a mounting failure. Therefore, you have to be very careful not to deform any external lead.

(5) When mounting a semiconductor device on a printed board by using a mounting socket, use an appropriate socket for each package.

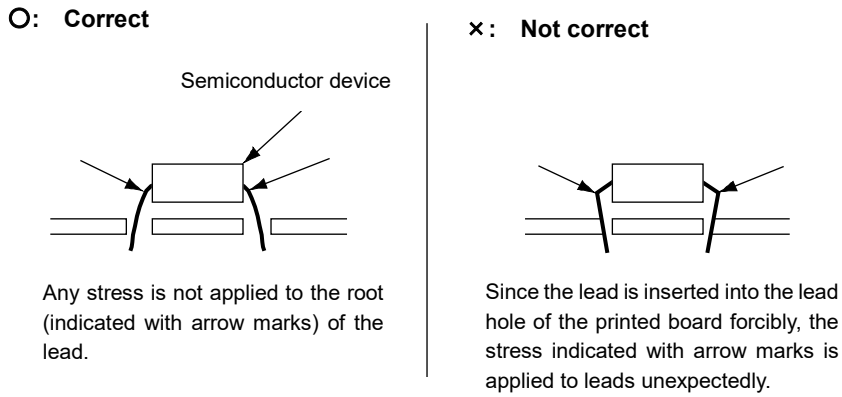


Figure 6-19 Notes on attaching a semiconductor device on a printed board

6.3.3 Washing Methods

In principle, flux must be removed after soldering. Otherwise, flux residue may affect the reliability of components, printed board wiring or solder junctions.

(1) Although ultrasonic washing is a highly effective for washing for a short time, you have to pay attention to the following items in order to prevent a device from being destroyed:

① Set proper frequency to be applied, output, and washing time.

② Prevent a device and a printed board from being brought in direct contact with each other or with the chassis of the ultrasonic washer.

(2) Do not rub marked surfaces during washing or while detergent has adhered to the device This may erase the mark. If washing time is long, the mark may disappear. Pay attention to the washing time.

(3) Even when washing a device with a solvent or just with water, washing should be performed so that other reactive ions such as sodium and chlorine will not remain in the device. Also, be sure to dry all of the parts completely.

(4) When using a solvent, be sure to take into consideration public environmental standards and safety standards.

6.3.4 Attaching a Heat Radiation Plate

Pay attention to the following points when attaching a heat radiation plate to a device.

(1) Use an appropriate attachment method so that any excessive stress will not be applied to the device.

(2) Pay attention to the flatness so that none of projections, recessions and burs will be formed on a heat radiation plate.
If a heat radiation plate is inappropriate, sufficient heat radiating effects may not be obtained, and the heat radiation plate forcibly attached may cause degradation of the characteristics or mechanical breakdown of the device.

(3) When there are two or more mounting parts on a heat radiation plate, first lightly pre-tighten all of the mounting parts, then tighten them by the regulated torque.

(4) Do not attach any heat radiation plate onto a semiconductor device after mounting the device on a printed board. Excessive stress may be applied to the semiconductor device depending on the state in which the device is mounted on the printed board. First attach the semiconductor device on the heat radiation plate, and then mount the device on the printed board.

(5) Thermal conductivity is generally improved when you coat the junction between a radiation plate and a semiconductor device with silicon grease. In this case, be sure to apply silicon grease there thinly and uniformly.

6.4 Notes on Handling of a Device in Case of Thermal Breakdown

A semiconductor device is formed by combining substances whose thermal properties are quite different from one another such as a silicon chip, plastic sealing materials and metallic lead frames including a copper one. Especially when plastic, which is a composing material, is exposed to high temperature, for example, during soldering, the moisture accumulated in the plastic is abruptly vaporized as a steam, and then causes a package to crack. The causes of failures such as delamination between the adhered portions of composing materials and disconnection of conductors brought about by repetition of heat stress are as follows.

(1) The mechanical strength is lowered significantly at high temperatures.

(2) Moisture in the air is absorbed and accumulated in the device.

This Section describes general precautions, particularly for mounting a product, to prevent this type of thermal breakdown of a device.

6.4.1 About Soldering

(1) Precaution to be taken when soldering

Semiconductor devices generally should not be left for a long time at high temperature.

When the soldering temperature is high and the soldering time is long during soldering, regardless of a used soldering method, hand soldering or reflow, the device temperature may rise and this may cause degradation or breakdown of the device. Therefore, soldering should be performed at a temperature as low as possible and within a time as short as possible.

(2) When soldering a through-hole device (THD) package with a wave soldering bath

With this method, the package lead pins to be soldered are dipped into the liquid surface of a wave soldering pod. However, note that the package may be damaged if the jet solder comes in contact with the package main body. Be careful not to bring the solder in direct contact with the package main body.

In addition, since the bottom of a board is heated by the solder heat when a wave soldering bath is used, the board warps due to the temperature difference between the front and the rear of the board.

If soldering is performed for the board warped in this manner, the board tries to be restored to its original state when it is taken from the soldering bath, so excessive stress may be applied to the leads and package, and then this may cause a soldered joint section to crack and damage the leads and the package.

Therefore, when using a wave soldering bath, soldering should be performed in a manner that does not cause any board to warp.

6.4.2 Notes on Mounting of a Surface Mount Device (SMD)

As a method for mounting an SMD on a board, the following methods for soldering by heating the entire package are frequently used: infrared reflow, air reflow, and vapor phase reflow.

Only the external lead terminals of a conventional THD are heated, while the entire SMD package is abruptly exposed to high temperatures, so you have to consider the following reliability problems: mold resin cracks and the moisture resistance deteriorates.

In addition, since an external lead terminal of an SMD is short, the interval of leads is narrow and the number of terminals is large due to high-density mounting, you have to be careful to handle it.

This Section describes the general precautions on mounting of an SMD.

(1) Notes on mounting of an SMD

When soldering is performed with a method for heating the entire device such as infrared reflow for a device whose mold resin has absorbed moisture due to long-term storage in the normal environment or storage in a high-humidity environment, the mold resin may crack or delamination may occur at the interface with a chip.

See Section “6.1.2 Notes on Cracking of a Package” when mounting an SMD.

(2) Deformation of an external lead terminal

If any external lead terminal is bent or floats, good solder connection with a board may not be obtained, and this may cause a mounting failure. Especially, pay attention to the flatness of external leads so that any terminal does not float during mounting.

In addition, even though only external lead terminals are controlled strictly when an SMD is mounted on a board, good solder connection may not be obtained if the board is not controlled sufficiently. Be very careful for warping of a board and the thickness and uniformity of cream solder also.

(3) Handling of taping parts

As for an SMD packed on a tape, static electricity is generated when the top cover tape is peeled from the carrier tape, and the SMD may become charged. This charge voltage increases as the speed at which the top cover tape is peeled becomes faster. High-speed tape peeling and rubbing should be avoided as much as possible to prevent electrostatic destruction.

(4) Other precautions

When coating a device such as an SMD with resin after mounting it on a board, moisture absorption may cause the leak current to increase depending on the coating resin, or the stress of the coating resin may also produce mechanical stress on the resin portion of the device. Therefore, you have to check the post-coating reliability thoroughly when selecting the coating material.

6.5 Notes on Product Specifications, Packing, Transportation and Storage

6.5.1 Product Specifications

6.5.1.1 Notes on Adoption of Semiconductor Devices

We make the utmost efforts to improve quality and reliability of our products, but due to the nature of semiconductor devices, a certain percentage of devices may malfunction or break down. When using our semiconductor products, customers have to design highly safe equipment and systems to prevent accidents resulting in death, injury or damage to property from occurring as a result of semiconductor failure on their responsibilities.

Note that when designing equipment and systems, the latest product specifications should be checked, and a product should be used within the product assurance range.

Semiconductor products are listed in catalogs and sold on the assumption that they will be used in general electronic equipment (such as home appliances, communications equipment, measuring instruments and office equipment). Be sure to consult our Sales representative beforehand if you have a plan to use our products for applications requiring special quality and reliability, or in equipment and systems (such as automobiles, traffic equipment, medical equipment including a life support device, a safety device, aerospace equipment and nuclear power control equipment) where a failure or malfunction of the product may directly threaten people's life or damage their bodies or their properties. Special consideration and selection are required for products that demand high reliability.

6.5.1.2 Absolute Maximum Rating

The destruction limit of semiconductor devices is specified in the [absolute maximum rating] and according to JIS C 7032, the absolute maximum rating is defined as [the limit value that must not be exceeded even for a second, and if the standard values are determined for two or more items, the limit value at which any two items can not be reached at the same time]. If the maximum rated value is exceeded even temporarily, it will lead to deterioration or destruction. And even if a device operated for a while afterwards, its service life would be extremely shortened. Figure 6-20 shows the relation among various types of guaranteed ranges of a device.

Therefore, when designing electronic circuits that use a semiconductor device, care must be taken not to exceed the absolute maximum rating of the device, including fluctuations of external conditions during use.

Since the absolute maximum rating varies depending on a device, it may vary among products of the same product family. Therefore, specification for each product shall be consulted before use.

Table 6-6 Example of items regulated with the absolute maximum rating

Item	Condition	Absolute maximum rating value	Description
Power supply voltage (V_{DD}) (V_{CC})	Temperature or other factors	Voltage value	Maximum voltage that can be applied between the power supply terminal and the ground terminal. 1. This is related to the endurance voltage of an internal element of the device, and the device may break down if the voltage exceeds this value. 2. CMOS devices may break down due to latch-up or injection of large quantities of hot carriers.
Input/output voltage (V_{IN}) (V_{OUT})	Temperature or other factors	Voltage value	Maximum voltage that can be applied between the input/output terminals and the ground terminal. This voltage generally cannot be larger than the power supply voltage. 1. Dielectric breakdown of elements parasitically configured on the input and output terminals may occur. 2. The input or output terminals may be broken down by a triggered latch-up.
Permissible loss (P_D)	Temperature or other factors	Power loss value	Maximum power consumption that can be allowed inside a device 1. The inside of an IC may be destroyed by heat generated during operation. 2. This value varies depending on the IC integration degree and the heat dissipation property of a package.
Storage temperature (T_{stg})		Upper and lower temperature limits	Allowable ambient temperature range during storage 1. The temperature is limited by the package materials and the intrinsic properties of a semiconductor.
Temperature of the junction (T_j)			Maximum tolerable junction temperature allowing a device to operate continuously

Note: Absolute maximum rating values are regulated by the individual specifications of each device.

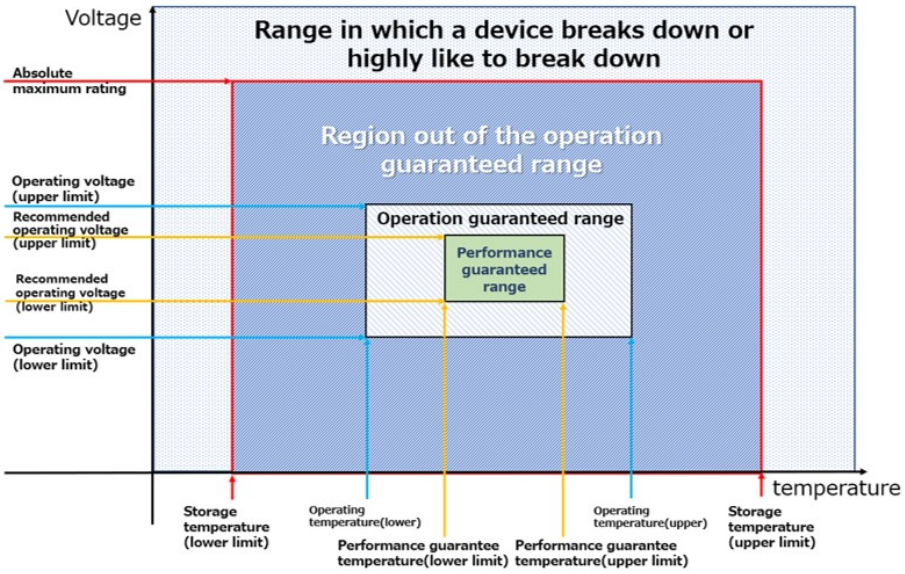


Figure 6-20 Relation among various types of guaranteed ranges

6.5.1.3 Operation Guaranteed Range

The operation guaranteed range refers to environmental conditions that can realize the operation/functions described in the product specifications. Some electrical and optical performance may not be demonstrated in devices for which performance assurance (characteristics assurance) range is individually defined.

Further, even when the maximum ratings are not exceeded, use outside the operation guaranteed range may prevent operational, functional, and performance (characteristics) specifications from being satisfied, and may lead to reduced reliability. Therefore, sufficient care should be taken for the system design.

6.5.1.4 Recommended Operation Conditions

The environmental range (temperature, voltage, frequency, etc.) in which products whose performance guarantee temperature is not specified especially in the product specifications can satisfy all the characteristic items is called recommended operating conditions.

6.5.1.5 Performance Guaranteed (Characteristics Guaranteed) Range

Some of our products have specifically defined environmental ranges (such as performance guarantee temperature and performance guaranteed voltage) in which the products can satisfy all items specified in the specifications (image quality, sound quality, sensitivity, noise, etc.).

Such products will satisfy all the performance criteria that are mentioned in the specifications only when all the environmental items are satisfied.

6.5.1.6 Derating

Traditionally, derating often referred to giving consideration in the designing process so that the power supply voltage is set to operate at the lower limit of operating voltage (in the case of positive voltage). At present, some devices have regulators built in so that their internal circuits are not affected by the supply voltage, and others including logic core of high-performance image processing engines have narrower power supply voltage range which should be strictly followed. If such devices are not used within the specified values, the signal timing margin with the peripheral device may be reduced.

As explained above, even for devices that are not suitable for use at the voltage lower limit, it is possible to prolong the life by lowering the operating temperature of the devices through proper designing of heat dissipation (heat exhaustion).

* In implementing measures against heat radiation (exhaust heat), temperatures should not fall below the lower limit temperature of recommended operating conditions.

It can be said that proper designing of heat dissipation (heat exhaustion) is the safest method of derating.

6.5.2 Notes on Packing, Transportation and Storage

Although a semiconductor device (referred to as a “device” hereinafter) maintains high quality and high reliability, improper handling, transportation, storage or use of the device may lead to its breakdown or degradation. The causes of breakdown or degradation of a device include electrostatic destruction during handling, package cracking during mounting due to moisture absorption into its package, mechanical breakdown due to shocks and bending of a lead. Items that should be kept in mind are described below.

6.5.2.1 Notes on Packing

The following three storage case packing formats are mainly used according to the device package shape and mounting format.

(1) Tray (2) Magazine (3) Embossed taping

The structure and materials appropriate for the quality of each package member are used for these packing formats to maintain the quality of a device.

Notes on each packing format are described below.

(1) Packaged in a tray

Two types of specifications of trays are provided: heat-resistant specifications and normal temperature specifications. Heat-resistant specification trays are marked with “HEAT PROOF” or indicate the heat resistance temperature such as “135 °C MAX.” When a device is to be baked (dried at high temperature), conform to the device baking conditions and perform baking within the heat resistance temperature range of the tray (125 °C MAX for trays marked with “HEAT PROOF”).

Any normal temperature specification trays cannot be baked. Therefore, when devices stored in a normal temperature specification tray are to be baked, these devices must be transferred to a heat-resistant specification tray. Anti-static measures should be taken to prevent ESD destruction before transferring devices from a tray. Also, be careful not to bump or press the electrode terminal against the tray to prevent the electrode terminal from being deformed.

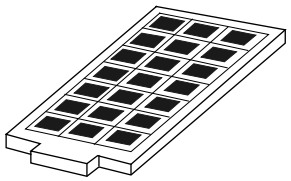


Figure 6-21 Tray

(2) Packaged in a magazine

The surface of a magazine is coated with a water-soluble antistatic agent. Therefore, note that the antistatic effect will be lost if the magazine gets wet with water or stored in a high-temperature and high-humidity place, or if a device is slid repeatedly.

In addition, magazines are not designed to be heat-resistant, so when devices are to be baked, transfer the devices to a metal magazine or other heat-resistant storage case. At this time, be careful to prevent a lead from being bent, and take the anti-static measures to prevent ESD destruction from occurring.

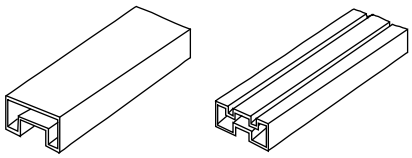


Figure 6-22 Conductive magazine

(3) Packaged in an embossed tape

A tape is not designed to be heat-resistant, so when devices are to be baked, transfer the devices to a heat-resistant storage case.

When transferring the devices, be careful to prevent an electrode terminal from being deformed and ESD destruction from occurring.

In addition, since the tape peeling strength is affected by the temperature and humidity of the storage environment, be careful to set a tape reel in a mounter.

The peeling strength measurement method conforms to “JIS C 0806-3:1999.”

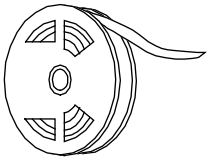


Figure 6-23 Tape

6.5.2.2 Notes on Transportation

Devices contained in trays, magazines and embossed tape are stored in our specified packing cartons, and then shipped to avoid the effects of external shocks during transportation, rainwater during storage, and contamination from the outside air.

If handling of freight is rough and a strong shock is applied to a packing carton during transportation, a lead of a device is bent or damaged in another way, and this may cause a failure during mounting of the device.

In addition, rough handling may also lead to breakage of an aluminum laminate bag used for moisture-proof packing. If the aluminum laminate bag is torn, a device may absorb moisture, and this may cause a problem that affect the device quality.

Therefore, pay attention to the following points during transportation.

(1) Although we make efforts to minimize shocks, vibration, humidity and other adverse effects applied to devices, application of excessive shocks or vibration may damage a device. Be careful to handle the device to reduce shocks and mechanical vibration.

(2) Be careful not to expose a device to direct sunlight or not to generate dew condensation.

(3) If a packaging box is received in a damaged condition, contact us without opening it.

(4) Instruction marks for handling are printed on packaging boxes as necessary. Be sure to follow these instructions for storage and transportation. Examples of these marks are shown below.

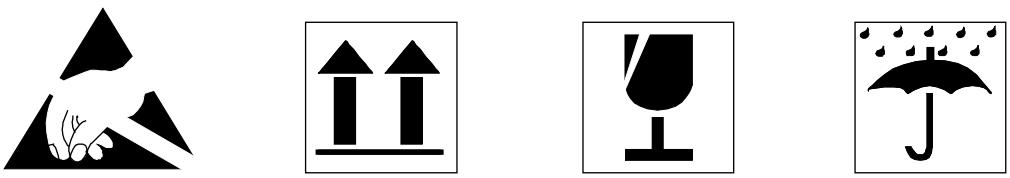


Figure 6-24 Example of instruction marks on a packaging box

- **Fragile: handle with care.**

  If you happen to throw or drop a packaging box when you handle it, the packaging material may be damaged or a device itself may be destroyed. Be careful to handle the packaging box.

● **This side up**

A packaging box should be placed facing the correct direction as indicated on the packaging box during transportation. If the packaging box is turned upside down or lean it against anything, unnatural force may be applied to the product and it may be damaged.

● **Keep dry**

When a carton box absorbs moisture, its strength is lowered drastically. Therefore, you have to prevent the carton box from being wet. Be careful not to allow a carton box to be wet especially while you are transporting it during rainfall or snowfall.

● **Static electricity: handle with care.**

This is not a caution to be followed during transportation, but it is indicated as a caution during mounting of a device on a set product.

6.5.2.3 Notes on Storage

The storage environment affects the quality of a device when you store it. Follow the items below to control the storage environment.

(1) Storage environment

Store a device indoors in an ordinary temperature ordinary humidity atmosphere [temperature (5 °C to 35 °C), humidity (30 % to 75 %)] as a guide.

(2) Storage period

The storage period of each packing format in the storage environment above is as follows.

Products packaged in a tray: 1 year from the delivery date

Products packaged in a magazine: 1 year from the delivery date

Products packaged on a tape: 1 year from the delivery date

The storage limit of each packing format is 1 year mainly because the solderability of a device is degraded, the effect of the water-soluble antistatic agent is degraded, the peeling strength of products packaged on a tape becomes unstable.

(3) Atmosphere

Do not store any device in a place exposed to direct sunlight, a place where corrosive gases are generated, or a place with a large amount of dust.

- A storage case (such as a magazine and a non-heat-resistant tray) may be deformed if it is exposed to direct sunlight.
- Corrosive gases cause an external lead terminal of a device to corrode and make the solderability worse.

(4) Temperature changes

Moisture condenses on a packed product in a place where the temperature changes abruptly. To avoid condensation, store semiconductor devices in a place where the temperature changes as little as possible.

(5) Avoid stacking packaging boxes or placing a heavy object on a packaging box as much as possible to prevent any load from being applied to a device.

(6) Store devices in a place not exposed to radiation, a strong electromagnetic field or static electricity.

(7) When storing devices for a long time, moisture-proof packing and packaging components must be changed to the other ones to handle them.

The solderability of a terminal of a device stored for a long time may degrade, rust may be generated on it, or its electrical characteristic may become improper. Contact us beforehand when long-term storage of devices is anticipated.

(8) Product packed in a moisture-proof package

As moisture-proof packing, a device whose quality may be affected by moisture absorption is packed in an aluminum laminate bag together with a desiccant and a humidity indicator in order to prevent a device from absorbing moisture during storage, and then this packing allows the device to be degasified and heat-sealed to block outside air and prevent moisture from getting into the bag.

If moisture gets into the moisture-proof package, a device may absorb moisture. If a device that has absorbed moisture is exposed to any high-temperature atmosphere such as the soldering process during mounting, a quality problem such as cracking of a package may occur. Moisture-proof packing is used to prevent such a kind of effects on the quality of devices.

Since a device begins to absorb moisture as soon as the moisture-proof package is opened, follow the instructions regulated according to the SMD rank to use the device within the specified period.

When this period specified according to the SMD rank passes, the device has to be baked again. Contact us for the baking time of each device.

In addition, a humidity indicator supplied with a device simply indicates the humidity condition inside a moisture-proof package. When the humidity indicated immediately after the moisture-proof package is opened exceeds 30 %, some trouble may have occurred. Contact us for this condition.

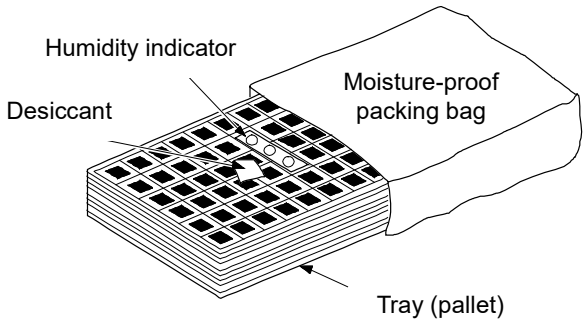


Figure 6-25 Example of moisture-proof packing

6.6 About the Thermal Management

This section describes the practical device thermal management. This document (Section 6.5 “Derating”) describes that using a device (strictly speaking “a chip”) by lowering the temperature is very important also from the point of view of reliability. (Note that the lowest temperature should be within the guaranteed range of the specification.)

While low-power consumption elements have been developed at a fast space, we shall not ignore the following facts: miniaturization of packages such as a CSP, increase of the circuit scale, and increase of power density per unit area, for example, caused by 3-dimensional high integration of devices including a multi-layer CMOS image sensor. The importance of thermal management has increased year by year under these circumstances.

Basically, thermal management of a device is performed with heat conduction, convection and radiation.

Since an optical device such as an image sensor is equipped with a light receiving part, any cooling mechanism such as a heat sink cannot be mounted on its upper section in the same manner as a system LSI. It is difficult to prevent dust from being stuck to the light receiving part even though forced convection performed with a tool such as fan is performed. The effective measures for heat dissipation cannot be taken easily in comparison with a general LSI package.

As the internal structure, an image sensor has a hollow structure, and there is air layer whose thermal conductivity is low between a chip and glass of the light receiving part. In addition, the distance between the chip and glass is so short that convection cannot be generated easily, and this structure cannot cause heat to be transferred toward the glass side.

Therefore, the main heat dissipation means for the image sensor package is heat exhaustion from the electrode on the rear side of the package to the mounting board.

Since image quality of especially a highly-sensitive image sensor may be affected by heat, you have to give appropriate consideration to countermeasures for temperature too.

When we perform thermal management, we have to consider not only heat exhaustion from the image sensor but also heating of the image sensor caused due to its peripheral parts. Partial heating of the image sensor caused due to the peripheral parts may generate non-uniform images.

6.6.1 Heat Dissipation Mechanism

As described above, heat transmission is classified into three heat transfer modes: heat conduction, convection and radiation.

The characteristics of each mode are described below.

6.6.1.1 Heat conduction

Heat conduction, which is described first, is a mode in which heat transfers from the high temperature side to the low temperature side via a substance when a temperature gradient is generated. Heat generated in a chip is diffused through an interposer board of the package to the outside, and then transferred to a mounting board through the solder joint.

Although heat conduction is a dominant heat transfer method as the heat dissipation method of a package, it is drastically affected with the size or thickness of a mounting board, the number of layers, a wiring pattern and so on.

Generally, the larger and thicker a board is, the more excellent its heat dissipation becomes. Copper, whose heat conductivity is high, is used in a wiring layer of a mounting board normally. Therefore, when many layers are used, heat can be diffused easily. Although a solid wiring layer is effective for heat dissipation, you have to consider the electrical characteristics that prevent the signal quality of input/output circuits from degrading when designing wiring normally, and confirm that a solid wiring shall not work as a capacitor when it is mounted on a device to induce any ESD destruction.

From the point of view of mounting reliability, a difference of residual copper rates of the front side and the rear side of a wiring pattern contributes to warp of a mounting board depending on temperature change, and when the residual copper rate of a wiring pattern is increased, the linear expansion coefficient of the board itself is increased (due to temperature change when mounted or in the market), and this may adversely affect the mounting reliability. When designing a mounting board, you have to consider these risks.

6.6.1.2 Convection

Convection is a mode in which heat is transferred by fluid such as air warmed by the surface of a high temperature object. When fluid such as air is warmed, its density becomes smaller, a floating force is generated, and then natural convection occurs. Convection occurs due to not only heat from the device package but also heat from a mounting board around the package and/or immediately below the package.

This convection changes even when a mounting board is located horizontally or vertically, or changes depending on the scale or shape of the space where gas circulates.

Enough space may not be able to be secured in a chassis because of miniaturization of a product caused by recent high-density mounting in many cases, and in such a case, heat dissipation allowed by convection cannot be expected. In addition, since a water-proof product into which any air intake and exhaust opening cannot be established cannot take in outside air or exhaust air into the outside, the heat dissipation measures for such a product with convection becomes more difficult.

When heat is dissipated by forcible convection of a fan, you have to consider influences on image shooting given by vibration and/or dust of the fan.

6.6.1.3 Radiation

Radiation is a mode in which heat is transferred through the following process: heat from the surface of an object is converted to electromagnetic waves such as visible light and infrared light, and then radiated. The hotter an object is, the higher this radiated energy becomes, and the energy is transferred from a high temperature object to a low temperature object and varies depending on the temperature of objects and/or their surface conditions. Although the other modes require another medium that transfers heat, radiation allows heat to be transferred even in vacuum. In comparison with the other heat transfer modes, radiation has a small influence on heat dissipation.

Finally, an image diagram indicating each heat transfer mode: heat conduction, convection and radiation is shown in Figure 6-26 below.

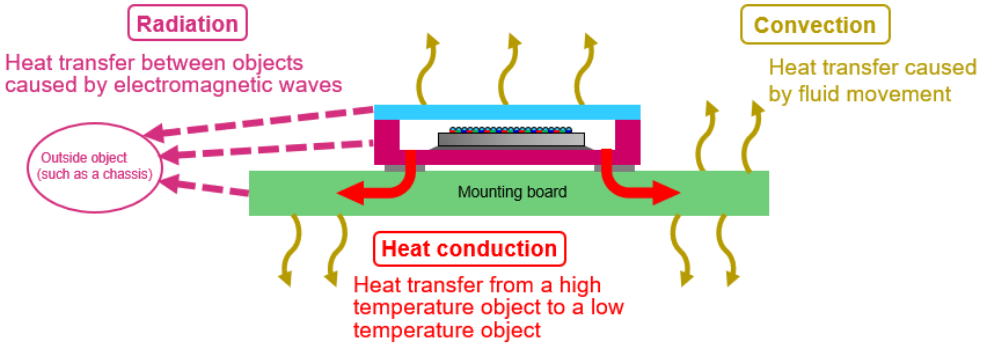


Figure 6-26 Heat transfer modes

6.6.2 About heat resistance

6.6.2.1 θ_{JA} (Heat resistance between Chip (junction) – Ambient environment (ambient))

A heat resistance value (θ_{JA}) between the chip temperature (T_J) and the ambient environment temperature (T_A) is the most generally used heat characteristic value of a package. When you use a θ_{JA}, you can compare thermal performances of different packages with one another.

Note that a θ_{JA} is not a fixed value and varies drastically depending on the measurement environment.

In particular, heat resistance is greatly affected by the size and thickness of a mounting board used for measurement and the number of layers of the board, and affected by convection around the package, the ambient environmental temperature or power consumption of a chip also.

Since the heat resistance characteristics of packages cannot be compared with one another in a uniform way due to the natures described above, the measurement environments (conditions) of these packages should be adjusted with one another so that they can be compared with one another correctly.

Measurement environment (conditions) has been standardized by JEDEC as the heat resistance evaluation method. When a θ_{JA} obtained by conforming to this standard is used, you can easily compare the heat characteristics of even packages whose manufacturers or shapes are different from one another.

However, it is very risky that a designer of the product uses θ_{JA} obtained under the standardized evaluation environment to calculate a T_J of the device. Note that a θ_{JA} is obtained under the particular environment.

As described at the beginning, a θ_{JA} is a value convenient to compare the heat characteristics of packages with one another, but it varies depending on the use environment. When a T_J is calculated with a θ_{JA} obtained under the environment standardized for an actual product, a T_J of a device may exceed the operating temperature range in the worst case.

6.6.2.2 θ_{JC} (Heat resistance between Chip (junction) – Topside surface of a package (case))

A heat resistance value between the chip temperature (T_J) and the temperature of the package topside surface (T_{Case}) is indicated with a θ_{JC}.

Generally, a value described as a θ_{JC} is obtained in conformance with the JEDEC standard in many cases, and it is measured under the ideal conditions: the bottom and sides of a package are thermally insulated so that all heat can be dissipated only from the topside of the package.

This measured value cannot be used as it is except when the package is equipped with a heat sink on its topside and has a cooling structure, and the heat sink is forcibly cooled down. This can be a reference value for checking the relation between the chip temperature and the heat sink to be cooled down. However, since devices other than a special one depend on the various heat dissipation methods, this value should be handled just as a reference value, and this can be applied to image sensor packages also.

Although it is difficult for customers to measure the chip temperature when designing their systems, the package surface temperature can be measured relatively easily.

When estimating the chip temperature (T_J) based on the package surface (case) temperature (T_{TOP}), a Ψ_{JT}, which is a heat characteristic parameter, is used. A Ψ_{JT} is obtained by normalizing a difference between the chip temperature and the package surface temperature by power consumption (P), and is expressed with the following expression:

$$\Psi_{JT} = (T_J - T_{Top})/P$$

6.6.2.3 θ_{JB} (Heat resistance between Chip (Junction) – Mounting board (board))

A heat resistance θ_{JB} value between the chip temperature (T_J) and the board temperature (T_B) is a value obtained under the ideal conditions also, that is the condition in which the devise topside and sides are thermally insulated and all generated heat is dissipated from the bottom side of a package only to the mounting board in the same manner as the heat resistance (θ_{JC}) value between the chip temperature and the package surface temperature.

A Ψ_{JB} is obtained by normalizing a difference between the chip temperature and the board temperature by power consumption (P), and is expressed with the following expression:

$$\Psi_{JB} = (TJ\text{-}TB)/P$$

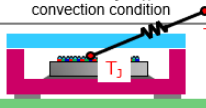
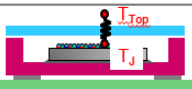
The relation between the chip temperature and the board temperature defined as Ψ_{JB} on the certain basis is an important parameter in the same manner as Ψ_{JT}, and can be said to be adapted to reality.

Both values are indicated with Ψ instead of θ because they are not heat resistance in the real sense of the term.

A Ψ value does not obtain any strict heat flow of the desired path in a process in which heat generated from a chip is dispersed into the package topside or a mounting board, but uses the total power consumption P of the device simply to obtain a Ψ_{JT} value and a Ψ_{JB} value.

Since heat resistance θ is supposed to be a symbol indicating resistance of a heat transfer path, θ is not used for a value obtained without considering the path. The same unit (°C/W) as heat resistance (θ) is used for this value, so you have to be careful not to confuse these values.

The heat dissipation paths are shown in the Figure 6-27 “Heat resistance and heat characteristic parameter types.

θ_{JA}	Ψ_{JT}	Ψ_{JB}
Heat resistance between T_J – T_A under the natural convection condition	Heat characteristic parameter between T_J- T_{TOP} under the certain ambient condition	Heat characteristic parameter between T_J- T_B under the certain ambient condition
		
$\theta_{JA} = (T_J - T_A)/P$	$\psi_{JT} = (T_J - T_{Top})/P$	$\psi_{JB} = (T_J - T_B)/P$

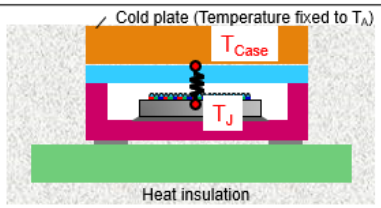
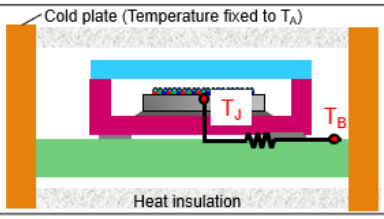
θ_{JC}	θ_{JB}
Heat resistance between T_J - T_{Case} under the condition where almost all heat is dissipated from the package surface	Heat resistance between T_J – T_B under the condition where almost all heat is dissipated from the mounting board
	
$\theta_{JC} = (T_J - T_{Case})/P$	$\theta_{JB} = (T_J - T_B)/P$

Figure 6-27 Heat resistance and heat characteristic parameter types

6.6.3 Heat dissipation varying depending on the chip size or package structure

Heat resistance θ_{JA} is a value obtained as a difference between the chip temperature per power consumption and the environmental temperature, and has the following characteristics according to the chip size and/or the package structure.

Although power consumption varies depending on the circuit scale or driving mode, power consumption per area is higher as the chip area decreases, and the heat density tends to become high at the same time. Therefore, a heat resistance value θ_{JA} indicates the larger value as the chip size decreases.

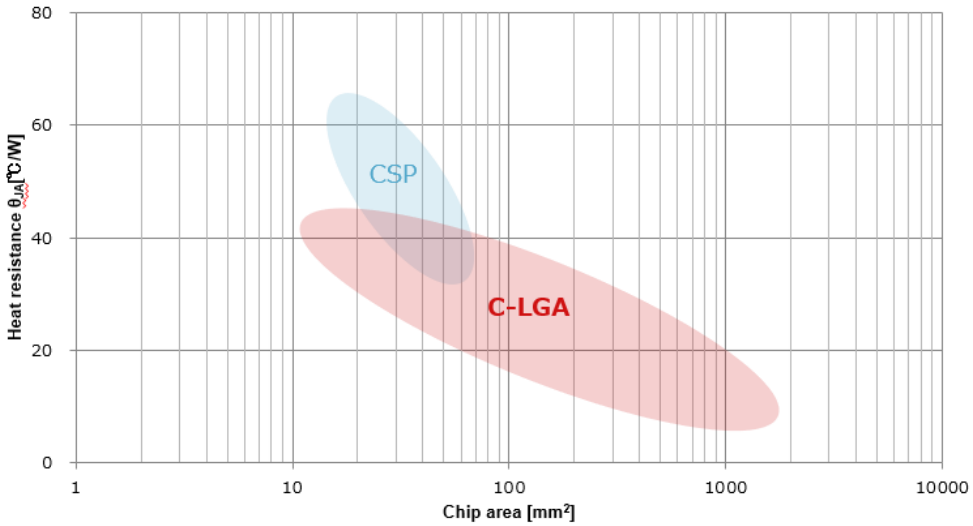
Especially the chip size of an image sensor is decided by not the circuit scale but the optical size mainly, and the chip size varies from a compact one to a large one.

Generally, a large optical size tends to be advantageous in thermal design, while this tends to increase mechanical stress because a terminal is easily affected by a linear expansion coefficient.

From the point of view of package composing materials, heat dissipation of a package using a ceramic board is better than that of a package using an organic board, and the former is excellent also as a heat dissipation function. From the point of view of package structure, since a CSP has a fewer dissipation paths similar with those of a ceramic package, its heat dissipation is disadvantageous structurally.

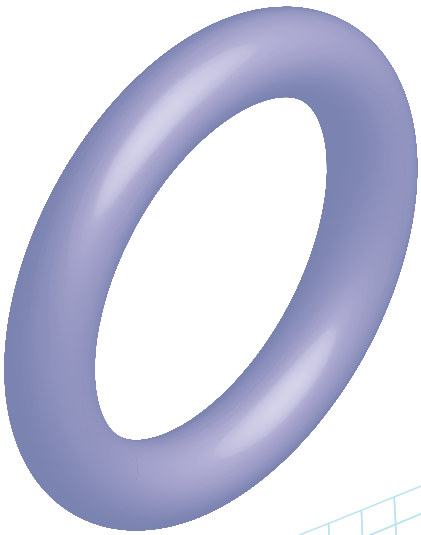
When you select a package, it is important to check a package totally, for example, based on the mounting reliability and the time to be elapsed until reflow as well as heat dissipation. Heat dissipation is one of the important factors.

A heat resistance (θ_{JA}) example of each chip size and package structure is shown in Figure 6-28 below.

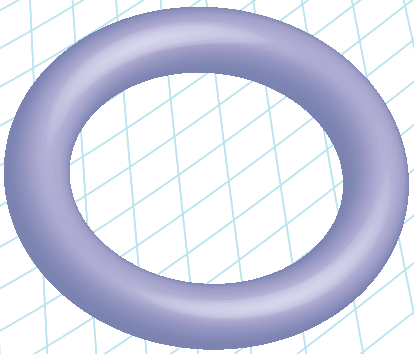


(Note) The values described above are calculated when natural convection is supposed to occur during heat generation at T_A = 25°C, 1W in conformance to JEDEC. Note that a heat characteristic value varies depending on a package size or the interposer board design specification.

Figure 6-28 Heat resistance (θ_{JA}) example of each chip size and package structure



Chapter 7 Notes on Each Product Category



Chapter 7 Table of Contents

7.1 Image Sensors

7.1.1 Nots on Mounting an Image Sensor

7.1.1.1 Notes on Mounting an Image Sensor during Soldering

An image sensor has a hollow package structure. When it is heated due to soldering, the pressure inside the package increases and its sealed glass-adhered portions easily delaminate. Therefore, the reflow mounting of an image sensor cannot be guaranteed generally.

Since the recommendable soldering conditions vary depending on the package materials, adhesive, and the package size, soldering should be performed within the range of the recommended conditions and according to the notes described in the individual product specifications.

(1) Recommended soldering conditions when using a soldering iron

It is recommended to pay attention to the following items to solder an image sensor.

- Use a 30-W or equivalent soldering iron with a countermeasure against static electricity, set its tip temperature to 350 °C or less, and solder each pin of an image sensor with the solder iron in 3 seconds or less.

  (The package temperature varies depending on a board and/or the work environment. Therefore, check the temperature at the following locations before performing soldering work.)

  ① Plastic or CerDIP packages : Glass-adhered portions 80 °C or less

  ② Laminated ceramic packages : Glass-adhered portions 95 °C or less

- Suppress the temperatures within the range described above when readjusting or removing an image sensor.
- When an electric solder-sucking device is used, an overvoltage may be applied to an image sensor due to surge at start-up. Use a device whose temperature control type is zero-cross ON/OFF type and ground it.
- Avoid local heating, rapid heating and rapid cooling.

(2) Recommended Conditions for Reflow

The following recommended conditions and notes should be observed for products whose respective specifications describe the recommended reflow conditions to solder them.

- Recommended reflow profile
- Storage conditions and time until reflow is performed after a deaeration package is opened
- Number of times of reflow operations

Note that when the solder inspection is performed with using X-ray transmission images, irradiation of a large number of X-rays may damage products due to increase in dark current or other factors.

7.1.2 Notes on Mounting an Image Sensor during Incorporation

7.1.2.1 Handling an Image Sensor during Mounting (Bonding)

- If a load is applied to the entire surface by a high rigidity component, bending stress may be generated depending on the flatness of the rear side of the package, and then the package may be broken. Therefore, use either an elastic load such as a spring plate or an adhesive to mount an image sensor.
- The adhesive may cause markings on the rear side to fade or become blurred.
- If metal strikes or rubs against the package surface, the package may chip or fragment, and then this may generate dust.
- As for products with leads, if the leads are bent repeatedly, the package may chip or fragment, and then this may generate dust.
- Note that use of an ultraviolet or infrared laser during mounting an image sensor may damage the image sensor.
- Observe the following limits when applying a static load to packages. In addition, do not apply a local load to the packages or a load to the inside of the glass area (hollow section).

Take special care for packages such as the following CerDIP or plastic-ceramic packages.

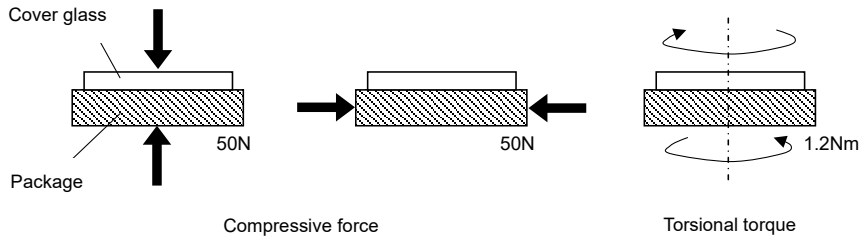


Figure 7-1 Allowable stress to a laminated ceramic package

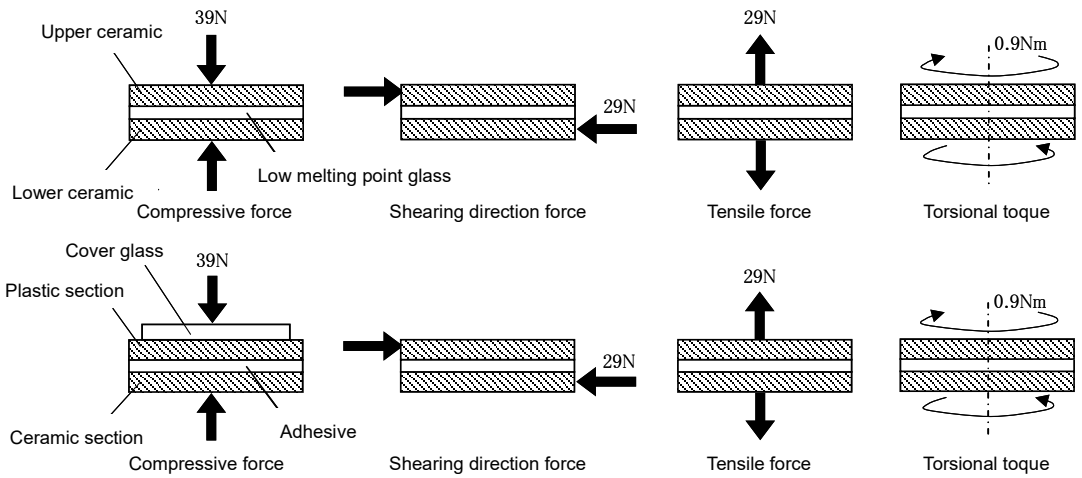


Figure 7-2 Allowable stress to a CerDIP/plastic-ceramic package

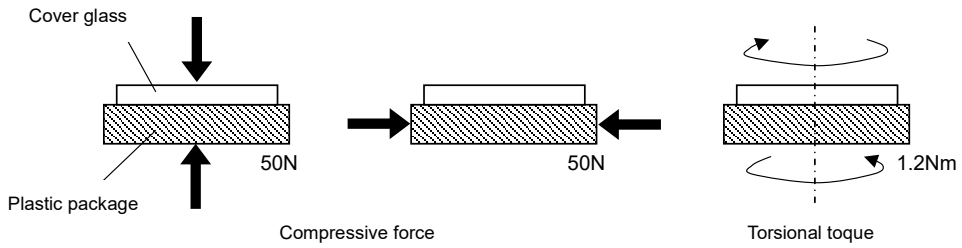


Figure 7-3 Allowable stress to a plastic package

7.1.2.2 Measures against Dust/Soiling

Image sensors are packed and delivered with taking care so that the element glass surfaces can be protected from dust and dirt harmful for use. However, glass surfaces should be cleaned by the following operations as required before using an image sensor.

Especially a product whose glass surface is coated with anti-reflection film is more easily scratched than plain glass, so that special care should be taken not to scratch the glass when it is cleaned.

(1) Perform tasks such as mounting of a lens system in a clean place (Class 1000 or less).

(2) Do not touch glass surfaces or bring any object into contact with glass surfaces. Use an air blower to blow dust or dirt off the glass surface when such a substance is stuck to the glass surface. (It is recommended to use ionized air to blow away dust stuck to glass surfaces due to static electricity.)

(3) Wipe away oil and fat stains with a cotton swab or similar tool moistened with ethyl alcohol so that any glass surfaces cannot be scratched.

(4) Store an image sensor in its dedicated case as a countermeasure against dust and dirt, and gradually heat or cool it when moving it to a room whose temperature is very different from that of the storage place as the measures against condensation.

(5) When protective tape is pasted on an image sensor at shipment, perform a measure against static electricity, and then remove the pasted tape immediately before the sensor is used.

Never reuse the protective tape.

(6) Although protective tape is designed to prevent glass surfaces from scratches, dust cannot be prevented from being caught between the glass surface and the tape is not protected. When an image sensor is stored for a long time, such dust cannot be removed easily or paste residue of the tape may easily remain in some cases. Long-term storage should be avoided whenever possible.

7.1.2.3 How to Remove Dust and Dirt

① As for the effective area and surrounding glass surfaces, incline the cotton swab (45° or less) and wipe away dust and dirt in the same direction as the lead arrangement as shown in Figure 7-4.

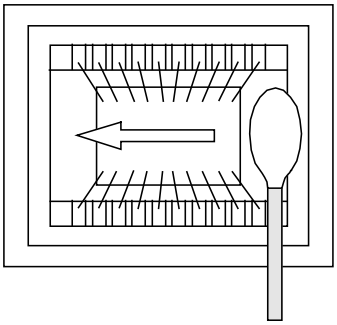


Figure 7-4 Wiping the glass surface

② As for the gap between the sealing glass and a package, keep the cotton swab straight up and wipe away the dust and dirt as shown in Figure 7-5.

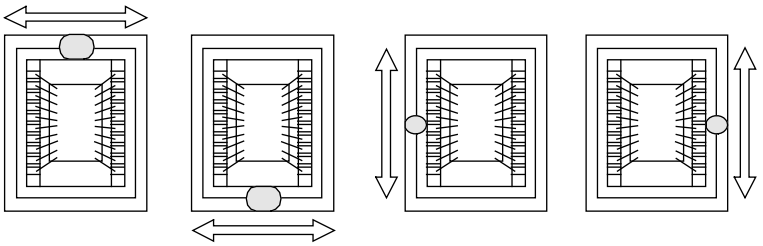


Figure 7-5 Wiping the sealing glass surface

[Notes]

- Do not wipe glass surfaces with a cotton swab if any dust or dirt is not stuck to it.
- In Step ①, do not allow the cotton swab to come in contact with the glass edges or the ceramic surface.
- Do not reuse any cotton swab.

7.1.3 Precaution for Handling of Products Packed in a Magazine

7.1.3.1 How to Take out a Product

When taking out products from a magazine, follow the procedure below to prevent any lead from bending due to dropping or other problems.

① Remove the rubber stopper. Be careful so that the products cannot fall from the magazine at this time.

② Incline the magazine by approximately 30° above a conductive mat and let the products slide slowly to take them out from the magazine. (Note that the products will be ejected out with great force when the magazine is inclined too much.)

Be sure to keep the take-out port outlet of the magazine at height of 5 mm or less from the mat while taking out the products. (Figure 7-6)

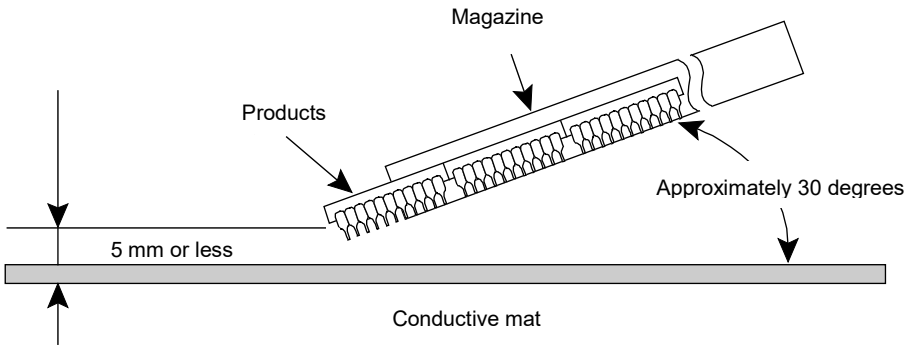


Figure 7-6 How to take out products from a magazine

7.1.3.2 Where to Store Fractional Products Less Than the Regulated Number after Opening a Magazine

After products are taken out, a magazine may contain fractional products less than the regulated number. When storing such a magazine, it is recommended to insert a rubber spacer of an appropriate length into the magazine and then attach a rubber stopper to the magazine to prevent the products from moving inside the magazine and being damaged, for example, due to shock. (Figure 7-7)

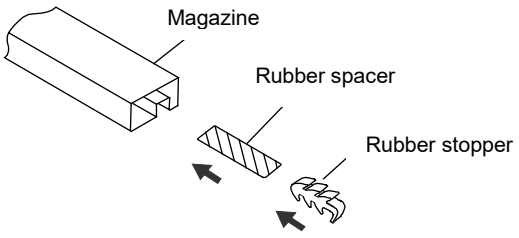


Figure 7-7 How to store fractional products in a magazine

7.1.4 Others

- Do not expose an image sensor to strong light such as ultraviolet rays and sunlight for a long time.

  It may affect a transmittance and/or color characteristics of the on-chip lens and color filter.

- Avoid storing or using an image sensor under sever conditions: a high temperature and high humidity because such conditions may adversely affect the transmittance and/or color characteristics.
- The imaging characteristics may be affected by noise or other factors when an image sensor is brought close to strong electromagnetic waves or magnetic fields during operation. Note that especially CMOS image sensors are easily affected.
- Note that as for an image of CMOS image sensor, when an infrared ray cut filter that has near infrared ray translucency is used, light leaks to an optical black region when a subject with high luminance is shot, and this affects the shot image.
- Our image sensor specifications do not assume use in environments whose radiation is higher than usual.
- White points are generated spontaneously in image sensors over time due to cosmic radiation. Generated white points should be compensated by using a white point complementing circuit.

7.2 Laser Diodes

7.2.1 Precaution for Handling a Laser Diode

Special consideration should be given to the following points to handle laser diodes unlike normal transistors and integrated circuits.

7.2.1.1 Eye Protection against Laser Beams

Take care not to allow a laser beam to enter your eyes in any condition. It is recommended to use safety goggles that interrupt laser beams when you perform inspection or measurement of a laser diode while oscillating it. Be sure to conform to the laser safety standards regulated in the IEC 60825-1 and Japanese Industrial Standards (JIS) C6802 “Safety of Laser Products.”

Warning labels such as those shown in the figure (Figure 7-8) below are described in the product specifications.

Refer to JIS C6802 for details.

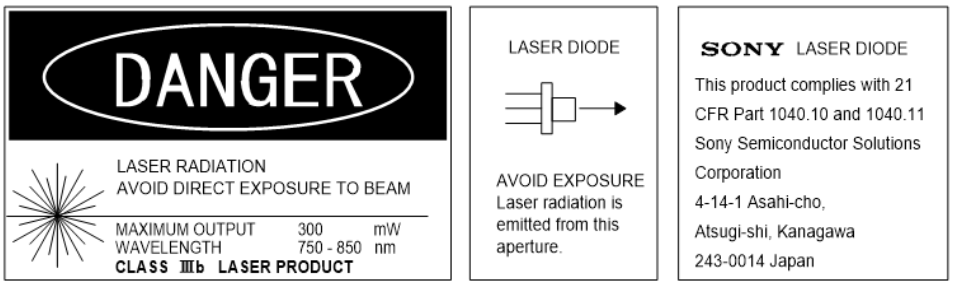


Figure 7-8 Examples of labels described in the product specifications

7.2.1.2 About Gallium Arsenide

Gallium arsenide (GaAs) is used in laser diodes (except for purple-blue laser diodes).
Although this is not a problem for normal use, it produces poisonous gas when it reacts with acids or steam. Therefore, never crush a laser diode, heat it to the maximum storage temperature or higher, or put it in your mouth.

In addition, the following methods are recommended to dispose of this product.

1) Request a qualified contractor to collect, transport and intermediately treat items containing arsenic.
2) Control the products until their final disposal as specially controlled industrial waste separately from general industrial waste and household waste.

7.2.1.3 Electrical Stress

Laser diodes (LD elements themselves) are one of semiconductor products not resistant to electrical stress. Therefore, handle them with great caution. It is recommended to monitor the optical output with using the photodiode built into the laser diode or an external photodiode, and to drive the laser diode by a constant power output within the range that does not exceed the recommended power output. When driving it by a constant current, pay attention to the temperature dependence of the I-L characteristics and take increase in power output at a low temperature into consideration to design your product.

We provide customers with consulting services in order to support measures against failures caused by electrical stress at their premises. Please contact our sales office when necessary.

(1) Overcurrent/surge current

The laser diode life becomes shorter as the operating optical output increases. The life cannot be guaranteed when it is used under conditions that exceed the recommended conditions. Use it within the range of the recommended conditions. In addition, note that if the optical output exceeds the absolute maximum rating even for an instant, the laser diode may be damaged, which may shorten the life or in the worst case may cause the laser diode to instantly stop oscillating. Of various kinds of damages caused due to electrical stress, the most common damage is caused by optical output exceeding the absolute maximum rating. The mechanism of this damage is as follows: “excessive light emission causes a light emitting end-face to get excessively hot, so that the structure of the light emission area is broken down.”

<Main causes of overcurrent and surge current>

a. Power supply problem (such as excessive overshoot of flowing current)

b. Adjustment errors (such as optical output adjustment knob overrun)

c. Electrical leakage or a potential difference between lines (such as current flowing just when a connection is made)

d. Static electricity (such as electric charges on the laser diode and electric charges on the human body or other surrounding objects)

e. Connection failures (such as chattering)

f. Work errors (such as circuit disconnection during energization)

g. Operating conditions (such as use under conditions that exceed the recommended conditions)

(2) Static electricity

Pay attention to static electricity because it causes surge current to flow to a laser diode.

When static electricity flows to a laser diode, the conditions and the damage mechanism are the same as those of overcurrent. Although the countermeasure varies depending on the situation, the basic approach to the static electricity is shown below when taking economic efficiency into consideration.

a. Prevent electric charges accumulated as static electricity from flowing to leads of a laser diode.

b. When static electricity cannot be prevented from flowing to a laser diode simply, implement protective countermeasures and limit the flowing current.

c. Ensure that a potential at the anode of a laser diode always becomes the same as that of a cathode for non-energizing time.

d. Suppress the generation of static electricity, or eliminate electricity.

   * Pay attentions to static electricity charged to especially the package of resin package products.

7.2.1.4 Contamination (dust and dirt)

(1) Note that when dust or dirt is stuck to the window glass of products, it may cause optical output to decrease or the light emission pattern to be deformed.

   a. Do not touch the window glass.

   b. Use an air blower or other non-contact method to remove dust stuck to the window glass.

   In such a case, be careful to avoid cross-contamination with mist or other substances contained in the blown air, scratches on the window glass left by contact with a nozzle, or ESD damage of the product due to static electricity generated by the air blower.

(2) Note that when corrosive gas or other harmful gases (such as outgas from the adhesive) is contained in the ambient atmosphere, it may have an adverse effect on products.

(3) The internal elements of open package products may be contaminated if any foreign substance (such as adhesive, solvent and dust) gets into the package. Be careful to prevent such a foreign substance from getting into the package. Contamination of the laser diode end face, photodiode light-receiving surface or other parts may cause the characteristics to deteriorate.

7.2.1.5 Mechanical Stress

When products are damaged by mechanical stress, leakage from the window glass or airtight parts may cause airtightness to decrease, or damage the laser element and internal connections. As a result, the product life may be significantly shortened or characteristics may deteriorate.

(1) Bending of an outer lead

Handle products having outer leads carefully to prevent their leads from bending. When the insulating glass at the base of the outer leads is broken, it may cause the airtightness to decrease.

(2) Removal of an outer lead

When an outer lead is pulled strongly from products having outer leads, the lead may fall out, or when it is pressed strongly, it may be dented. In particular, to pull out a laser diode already mounted on a board, the outer leads should be completely freed before you pull it out.

(3) Damage of a package

When strong force is applied to the laser diode package, it may cause bonded materials to delaminate, or the package to be deformed, chipped or cracked.

(4) Damage of the window glass, lens or other glass parts

When strong force is applied to the window glass, lens or other glass parts of laser diodes, it may scratch, soil or crack such a part or cause it to drop off from the laser diode. In addition, when strong force is applied to the package, the package may be deformed and the window glass, lens or other glass parts may be cracked, and then drop off from the package.

(5) Damage of an internal element

When tweezers or other tools gets into the inside of open package products, the internal elements may be damaged in some cases. So, take care not to allow these items to get into the inside of the package.

7.2.1.6 Thermal Stress

(1) Operation under a high-temperature environment

The higher the case temperature is when a laser diode is used, the shorter the life of the laser diode becomes. Note that the life cannot be guaranteed when it is used under temperature conditions that exceed the recommended conditions.

(2) Heating due to soldering

Note that excessive heating during soldering may cause the internal elements of laser diodes to deteriorate.

7.2.1.7 Condensation

(1) Optical path failure

When laser diodes are moved abruptly, for example, from a low-temperature environment to a room temperature or high-temperature environment, condensation may be temporarily generated on the glass surfaces. Note that this may cause the product characteristics to deteriorate temporarily or stains to be stuck to the window glass surface.

(2) Electrochemical reactions

When open package products operate in the condensation condition, electrochemical reactions of the internal element(s) may cause the product characteristics to deteriorate. Avoid the use of these products in the condensation condition.

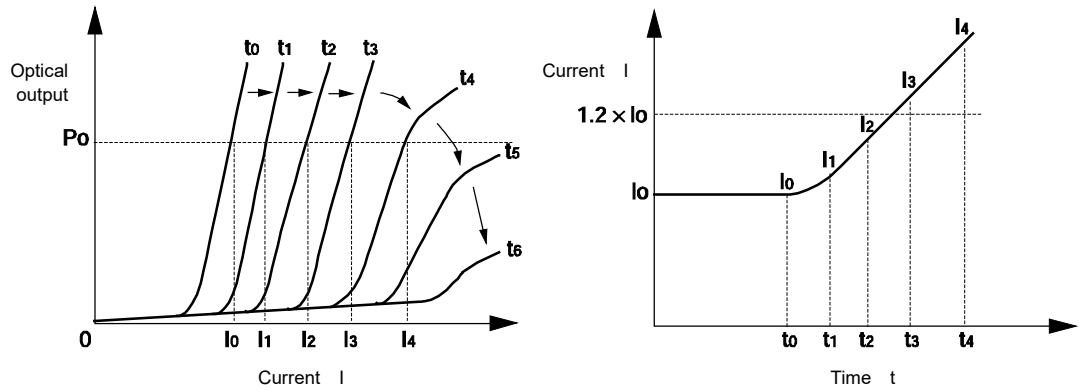
When you use a laser diode, read this Section before using it to operate it safely and properly.

7.2.2 Reliability of a Laser Diode (LD)

7.2.2.1 LD failures

When laser diodes, which are light-emitting elements also, are operated, increase in the current that does not contribute to light emission causes the light emission characteristics to change over time. Among these characteristics, the element life is generally defined by the time-dependent change in optical output vs. operating current characteristics, which have a big influence on the drive circuit. This is shown in Figure 7-9 (a). When automatic power control (APC) driving that keeps optical output constant is performed, light cannot be emitted at the constant optical output P0 even at time t5.

For example, when the life of a laser diode is defined as the time period when the operating current becomes 1.2 times the initial value, the laser diode is supposed to have malfunctioned between t2 and t3 as shown in Figure 7-9 (b) below. However, as shown in Figure 7-9 (a), this does not mean that the laser diode is no longer able to emit light.



(a) Time-dependent change in the optical output vs. operating current

(b) Time-dependent change in the optical output vs. constant operating current

Figure 7-9 Time-dependent change in the operating optical current characteristics

7.2.2.2 Degradation Factors

Reliability of a laser diode is closely related to the operating temperature, and the degradation speed (increase in the drive currents per unit time: Δlop/Δt) rises exponentially with the operating temperature. This relationship can be expressed as follows:

$$\tau \propto \frac{\Delta Iop}{\Delta t} \propto \exp\left(\frac{-Ea}{kT}\right)$$

Ea : Activation energy (eV)
k : Boltzmann constant (8.616×10^{-5} eV/K)
T : Absolute temperature (K)

For example, degradation of an AlGaAs laser diode is obtained based on the relation between the temperature and the driving current increase rate as shown below 1):

Ea ≒ 0.7 eV

The life is lowered to approximately 1/2.2 relative to a temperature rise by 10 °C at vicinity of a room temperature. When a laser diode is mounted on especially a small device, you have to sufficiently consider thermal design to suppress temperature rise of the laser diode. Such a degradation dominating the long life is referred to as gradual degradation or wear degradation. This wear degradation is accelerated when optical output becomes large. Therefore, it is important to use a laser diode below the upper limit of the optical output described in the specifications in order to obtain sufficient reliability.

"End-face degradation" caused by surge current or overcurrent flowing to a laser diode occurs frequently while the laser diode is being used. When the current is raised to increase the optical output of a laser diode, the optical output is lowered abruptly and a laser diode is irreversibly damaged. This type of degradation is also referred to as Catastrophic Optical Damage (COD), and it is caused when high optical output density operation melts a part of the end-face of the laser diode instantly to generate crystal defects.

Since laser diodes have a 1 GHz or more high-speed response and are instantly damaged, surge breakdown is one of failure mechanisms unique to laser diodes. In order to avoid the COD failure caused due to surges, it is necessary to prevent even momentary excessive optical output from being generated by a momentary overcurrent entering from the power supply or surges. In addition, it is already confirmed that the operating life becomes shorter thereafter even if a relatively weak surge is applied and the initial deterioration of the laser diode characteristics is just small. Therefore, be careful about such a weak surge also.

7.2.2.3 Methods for Estimating Life

The life of laser diodes is different from that of other semiconductor devices, and is sometimes expressed with using the mean time to failure (MTTF). The method for obtaining the MTTF is described below.

Since the life of laser diodes generally follows a Weibull distribution, the MTTF is expressed by the following expression, where η is the characteristic life (scale parameter), m is the shape parameter, and a gamma function is used.

$$MTTF = \eta\Gamma\ (1+1/m)$$

η and m can be obtained by plotting the failure time on Weibull probability paper.

Note that when m = 1, $\Gamma\ (2) = 1$, so the MTTF is equal to the characteristic life η.

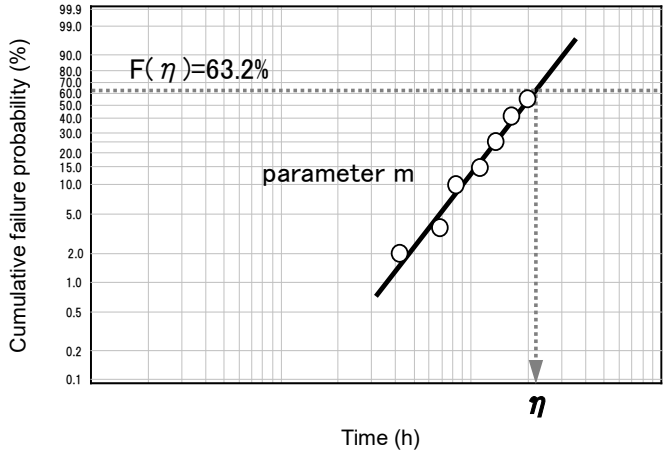


Figure 7-10 Weibull plotting: how to obtain m and η

7.2.2.4 Failure Analysis

When a trouble occurs at a laser diode, its cause is investigated totally by checking the electrical characteristics and optical characteristics and observing the laser diode with optical microscopes and SEM.

When current flows to a laser diode, the stripe portion emits light. Therefore, the cause of the failure is generally estimated by observing this emitted light. The laser diode end-faces which emit light and the entire stripe portion from which the electrode and semiconductor layers shielding light from the inside of the laser diode are removed are to be observed.

This section introduces failure analysis methods that use the light-emission characteristics different from common semiconductor devices.

(1) Analysis of light emission of the laser beam emission end surface

"End-face degradation" caused by surge current or overcurrent flowing to a laser diode occurs frequently while the laser diode is being used. This degradation is also referred to as Catastrophic Optical Damage (COD), and occurs when high optical output operation melts a part of the laser diode end-face instantly and generates crystal defects. Since this melted portion absorbs light, this is observed as degradation of the laser diode characteristics. The following failures are observed frequently as a result: the operating current needed to obtain a certain optical output increases (large Iop), the rated output is not produced, the laser diode does not oscillate, an extremely large overcurrent flows to a laser diode, and any current cannot flow.

A low current of several mA is flowed to the laser diode to make it emit light, and the light intensity distribution at the light emission end surface is observed (observation of the near field pattern). Normal laser diodes present a Gaussian distribution as shown in Figure 7-11. During laser oscillation, the light density is highest in the center of the light emission area of the light emission end surface, so that crystal is melted at this location. Therefore, when the center of the near field pattern appears dark or forms a double peak or when the pattern

appears divided into a number of peaks, this indicates that a surge or overcurrent has been applied to the laser diode, a light absorbed area is generated near the center of the light emission area, and the end-face is degraded. (Figure 7-12)

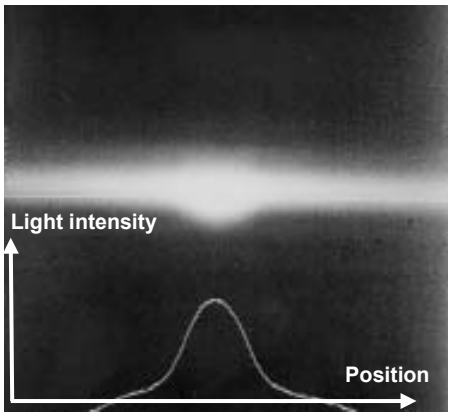


Figure 7-11 Normal end-face light emission pattern

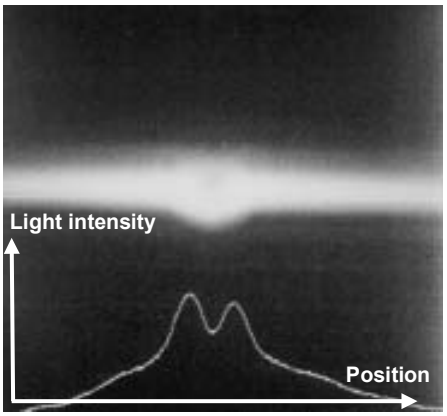


Figure 7-12 Degraded end-face light-emission pattern

(2) Analysis of light emission from the entire laser diode surface

As for test samples where abnormalities are not found by observing light emission from the end-face or a laser diode chip containing a defect, the entire stripe must be analyzed. The cathode luminescence method allows observation of the entire stripe of a malfunctioning laser diode. To do so, remove the electrode layer and the semiconductor layer both of which shield the light by using chemical etching in order to observe light emission from the light-emitting layer inside the laser diode chip. Then, make the light-emitting layer of the laser diode emit light by irradiating it with an electron beam instead of flowing current to it. If the light-emitting layer contains a Dark Line Defect (DLD), it is possible to accurately know the DLD shape, orientation and resolution. Figures 7-13 and 7-14 show cathode luminescence images of a laser diode: a crystal defect called a DLD has been generated near its end-face.

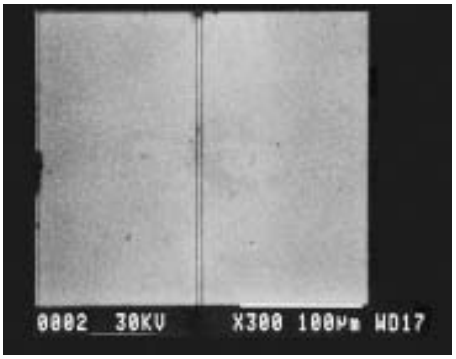


Figure 7-13 Cathode luminescence image of a laser diode with a crystal defect near the end-face

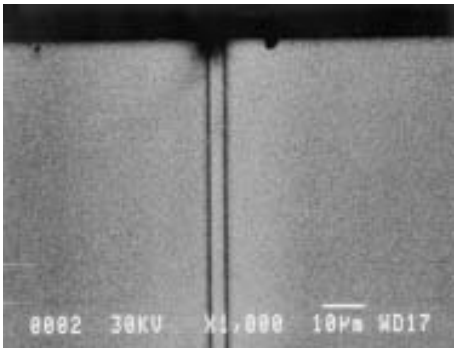


Figure 7-14 Enlarged image

References:

1) R. L. Hartman and R. W. Dixon, “Appl. Phys. Lett. 26,” p. 239-242 (1975)

7.3 Liquid Crystal Display (LCD)

7.3.1 LCD Optical Reliability

7.3.1.1 Overview

Our LCD products include high-temperature polysilicon TFT-process LCDs mainly used for video camera viewfinders or liquid crystal projectors and silicon reflective type LCDs (SXRD) used for digital cinema projectors or simulation projectors. External stress factors impairing the reliability of these LCDs include not only general stress factors for semiconductors but also existence of light emitted to LCDs. As for a projector LCD, the light density of the light incident on the panel is extremely high, and strong light stress is applied to it for a long time. Therefore, a reliability problem may occur due to the incident light depending on how to use it. This section describes the optical reliability of LCDs mainly used for projectors.

7.3.1.2 Deterioration Mechanisms

Reliability problems and characteristics problems caused by light incident on an LCD for a projector cause two main phenomena to occur. The first phenomenon is as follows: photochemical reactions caused by optical energy absorbed with the used organic materials change the molecular structure of the organic compounds. The other phenomenon is as follows: electron-positive hole pairs are generated after light sneaking in the pixel transistor is absorbed by the TFT bulk, and then these pairs change the pixel potential.

(1) Deterioration caused due to photochemical reactions of the organic materials

Changes of the molecular structure of the organic compounds made as a result of light irradiation are supposed to be the following phenomenon: optical energy absorbed by the organic compound causes a photochemical reaction, and this dissociates the organic bonds. As the photochemical reaction of the organic compound progresses, the picture quality may be affected by the orientation degradation of the liquid crystals or the generation of ions.

The rate of the light-induced chemical reaction can be indicated by the function f (λ) of the absorbed energy that contributes to the photochemical reaction, the function f (P) of the incident light quantity and an Arrhenius expression indicating the temperature dependence of the chemical reaction rate.

$$L = A \cdot f(\lambda) \cdot f(P) \cdot \exp\left(\frac{Ea}{kT}\right)$$

The photochemical reaction rate is proportional to the amount of optical energy absorbed. Therefore, the reaction rate becomes higher as the incident light quantity increases or as more light within an ultraviolet light region with high photon energy is absorbed.

The light resistance life can be extended by cutting as much as possible of the unnecessary light within an ultraviolet or near ultraviolet region from the wavelength component of the light incident to the LCD panel, or by lowering the panel temperature to suppress the photochemical reaction.

(2) Signal charge fluctuation caused by light absorption with a pixel transistor

A pixel transistor making up one pixel of the LCD is shielded from light with metal layers on the top and bottom to prevent the characteristics from fluctuating due to light incident on the transistor. However, when diffracted light generated at the edges of the light shielding film or light incident on the panel from a diagonal direction sneaks in the transistor from the light shielding metal and then gets into the TFT portion due to reflection, electron-positive hole pairs are generated due to light absorption by the bulk, and causes the following phenomenon: the pixel potential changes.

When light is made incident on a pixel transistor, and then absorbed by the bulk of the transistor, electron-positive hole pairs are generated inside the bulk by photoelectric conversion. As for the electron-positive hole pairs generated in the depletion layer region on the pixel electrode side of the TFT, the electric field inside the depletion layer causes the electrons to migrate toward the pixel electrode side and the positive holes to migrate toward the drain side. When electrons migrate toward the pixel electrode side, the pixel potential on which the video signal is written fluctuates and the electric field applied to the liquid crystal changes. If the incident light intensity increases, the number of the generated electron-hole pairs increases, and this causes the quantity of electrons flowing to the pixel electrode to exceed a certain level, the normal hold voltage cannot be maintained and this may make the picture quality deteriorate in some cases.

This phenomenon is not progressive, so it does not affect the long-term reliability. However, it is an index indicating the characteristics limit with respect to the quantity of light incident on the LCD.

7.3.1.3 Light Resistance Evaluation Method

Figure 7-15 shows an optical system of a device used for light resistance evaluation of an LCD for a projector. A high-pressure mercury (UHP) lamp generally used in projectors is used as the light source, and changes in the optical characteristics are evaluated by using the condensing lens to irradiate the LCD panel with light so that the condensing lens can condenses light over the LCD panel surface uniformly.

The main acceleration factors of the light resistance test are the irradiation light quantity and the panel temperature, and each of them can be controlled.

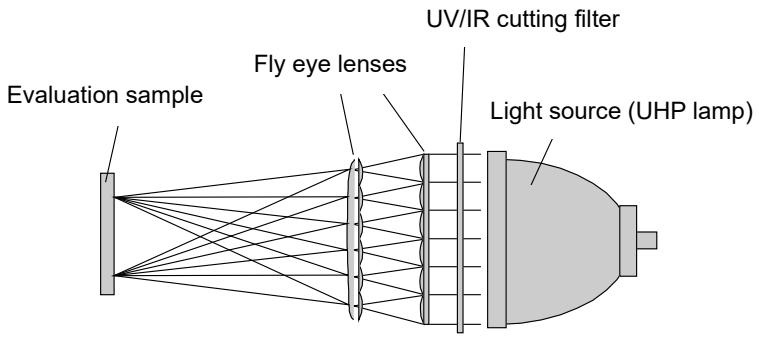


Figure 7-15 Configuration of a light resistance evaluation device

7.3.2 Handling an LCD

7.3.2.1 Electrostatic Countermeasure

Display elements of a TFT-LCD can be easily damaged due to an electrostatic discharge. Be sure to take the following antistatic measures.

a) Use non-electrostatic gloves, or simply use bare hands to work.

b) Use a wrist strap when directly handling an LCD.

c) Do not touch any electrode portion of an LCD.

d) Wear non-electrostatic clothes and electroconductive shoes.

e) Spread a conductive mat on the work floor and worktable respectively.

f) Keep a panel away from any charged materials.

g) Use ionized air or similar tool to discharge the panel when handling it.

7.3.2.2 Antifouling Measures

a) Perform a task for an LCD under a clean environment.

b) When an LCD is delivered, a glass plate equipped with a protective sheet is pasted on the panel surface. Take appropriate antistatic measures, and then peel off the protective sheet carefully so as not to damage the glass surface immediately before using the LCD.

c) Do not touch the glass surface because the surface can be easily scratched. When you have to clean it unavoidably, gently wipe the glass surface with a clean-room wiper that is moistened with isopropyl alcohol and hardly causes dust. Be careful not to leave a stain on the surface.

d) Use ionized air to blow dust off the glass surface when it is stuck to the glass surface.

7.3.2.3 Notes on Light Resistance

As described in Section 7.3.1.2, the organic materials used in LCD panels such as liquid crystal may degrade due to photochemical reactions. As a result, the display characteristics may change irreversibly in some cases. When the amount of light is constant, the dominant factors that determine progress of the photochemical reactions are light on a side of a shorter wavelength (characteristics of a UV cut filter) and temperature. Mount an appropriate UV cut filter (half-width wavelength: 434 nm or more is recommended) between the light source and the LCD panel to restrain progress of the photochemical reactions.

In addition, use an appropriate IR cut filter to lower the temperature of the LCD panel as much as possible and pay enough attention to cool the LCD panel. Irradiate light only after driving the panel to stabilize the initial drive operation with sufficient care also.

7.3.2.4 Other Precautions for Handling

a) Avoid holding a flexible board by the hand or avoid applying any force to a flexible board by twisting or bending it because its connecting portion can be damaged easily when it is twisted.

b) Do not drop any panel.

c) Do not apply any force to an outer frame or a panel by twisting or bending it.

d) Keep panels away from a high-temperature object such as a fire.

e) Do not soak any panel in water or other solvents.

f) Avoid storing or using an LCD under sever conditions such as a high temperature or high humidity because these conditions may affect its characteristics.

g) The minimum bending radius of a flexible board and the screw tightening torque for mounting a panel are regulated for each device respectively. For details, see the product specifications.

h) Use appropriate filters to protect a panel.

i) Do not apply any force to locations (such as a parting plate) other than the panel mounting holes.

j) Be sure to dispose of an LCD as industrial waste in accordance with the related laws and regulations.

7.4 Quality Assurance of Bare Dies

Quality specifications for bare die products shall be decided together with the customer in accordance with “JEITA EDR-4703A: Quality Guidelines for Bare Dies.” Items that should be kept in mind when purchasing bare die products are described below.

(1) Assurance of the electrical characteristics and reliability verification

Assurance of the electrical characteristics and reliability verification of bare dies are categorized as shown in Table 5-1 regulated by EDR-4703A. In principle, we ship bare dies categorized as Probed Dies (PD). When you want to purchase bare dies categorized as Know Good Dies (KTD), we have to sufficient consultation with you based on the specific demands for assurance and verification items.

Please understand that significant investment in facilities (such as final inspection equipment and burn-in equipment) is required to satisfy the characteristics assurance and reliability verification requirements equivalent with those of a package product as for KGDs and this is technically difficult also.

Table 7-1 EDR-4703A Bare die reliability verification and characteristics assurance matrix

Functional test / Reliability	Simplified test (DC and simplified function tests only)	Assurance covers most of the functions except analogue characteristics, at-speed performance, and functional verification over the assured operational temperature range.	The equivalent test to that of the packaged device (Design-based assurance is also acceptable.)
EFR of the bare die is verified to be similar to that of the packaged device by conducting the equivalent lifetime test to the packaged device.	N/A	KTD (Level 2)	KGD (Level 1)
Lifetime test or EFR verification has not been performed. Or EFR is inferior to that of the packaged devices.	PD (Level 3)	KTD (Level 2)	KTD (Level 2)

Note 1) KGD is abbreviation of Known Good Die, KTG is Known Tested Die and PD is Probed Die.

Note 2) The table shown above is subject to change, so be sure to check the JEITA technical standards.

(2) Other main points of attention

① When storing bare die products, the atmosphere of the storage and the allowable number of storage days are restricted both in the unopened condition and after the package is opened. Be sure to satisfy the conditions prescribed in the specifications.

② Physical damage such as scratches, contamination, and electrostatic discharge have fatal effects on the quality of bare die products. Be careful to handle the bare die products.

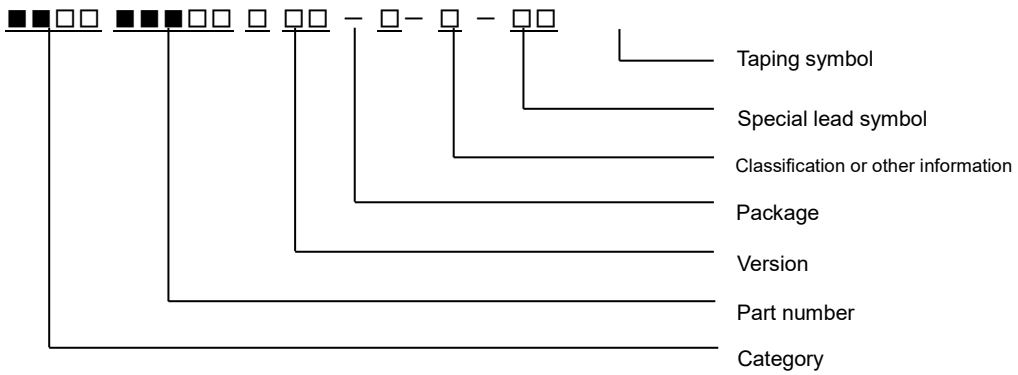
③ Bare die products cannot be marked for identification like package products. This makes it difficult to clarify the affected range if a quality problem occurs. It is desirable to establish a management system or other means capable of ensuring traceability at your site also.

④ The returned product format, analyzable range and other items concerning defective products shall be agreed upon through prior consultation.

7.5 Product Names and Lot Indications

Product names and lot indications of our products are regulated as follows.

(1) Product Name Indications



■: Required

□: Optional

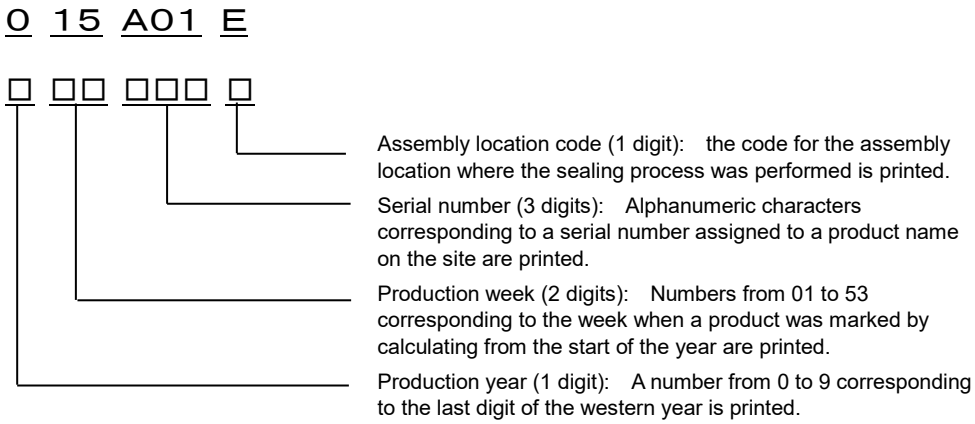
Table 7-2 Category table

Category	Description
1T	Super-mini varicap, super-small mini varicap, mini varicap
2SK	Silicon transistor, FET
3SK	MES FET
CXA	Bipolar/MOS analogue
CXB	Bipolar digital
CXD	MOS logic, MOS gate array, ASIC microcomputer
CXG	GaAs integrated circuit
CXJ	Other module products
CXK	Products related to memory
CXM	Multi-chip module
CXN	Bluetooth module product, Transfer JET module product and its related product, optical communication module product and its related product
CXP	16-bit microcomputer (SPC-A1), products designed for special use, Mask ROM version, 4-bit, 8-bit or 16-bit microcomputers (SPC900) other than those listed on the left side
CXQ	Second source microcomputer
CXR	Products related to RISC
DCX	X ray sensor

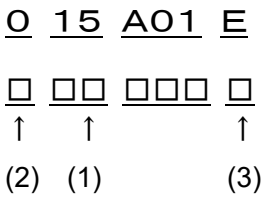
Category	Description
DM	Magnetoresistive element
DS	Optical engine
DS-	Service parts for an optical engine
ECX	Organic EL
GXB	GPS module product
ICX	CCD image sensor
ILX	CCD linear sensor
IMX	CMOS image sensor
ISX	CMOS image sensor SoC (System On Chip)
IU	CCD lens module/CMOS lens module
IUS	Camera module
IWF	Wafer board to be supplied for a fee
JSX	Mounting business products
LCX	High-temperature process LCD
MCB	Camera module (Sensor + ISP)
MXC	MEMS chip
MXL	MEMS module (optical system)
MXR	MEMS module (RF system)
MXS	MEMS module (sensor system)
PHD	Photodiode
RCX	Parts related to a high-temperature process LCD
SAS	Optical communication module
SGH	HEMT
SGM	MES FET
SLD	Laser diode (basic)
SLG	Laser diode (multi-beam VCSEL)
SLK	Optical integrated element such as a laser coupler
SLL	Parts related to a LED
SLN	Laser diode (frame)
SLP	Photodiode using a compound semiconductor
SLU	Laser diode (advanced)
SXRD	Reflection type LCOS

(2) Lot indications

A lot number is composed of seven digits representing the year and week of manufacture, a serial number and a code indicating the assembly location.



When seven digits cannot be printed due to the printing space, some of the printed characters are omitted according to the following priority.



(1) Omit the week of manufacture.

(2) Note the year of production by using a binary code.

(3) Omit the assembly location code.